Radiation Characterization of a Dual Core LEON3-FT Processor

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***Abstract*— A dual core 32-bit fault-tolerant SPARC™ V8/LEON3-FT processor has been developed and manufactured by Ramon Chip Ltd and Aeroflex Gaisler AB and characterized for radiation effects. It is designed with Aeroflex Gaisler's intellectual property and implemented with Ramon Chip's RadSafe™ radiation-hard-by-design library in a commercial 0.18µm shallow trench isolation CMOS process. Radiation test results for total ionizing dose, single event latch-up and single event upset data with correction/data-restore methodologies are reported, demonstrating its suitability for operating in a space environment.**

***Index Terms*— Single Event Upsets, Total Ionizing Dose, Processor, Error correction.**

I. Introduction

Radiation effects can be a significant problem for devices operating in a space environment. Soft errors, in particularly, is a problem for processors because of their complexity.

In a commercial 0.18µm shallow trench isolation CMOS process, Ramon Chip Ltd together with Aeroflex Gaisler AB has developed and manufactured a dual core version of the LEON3-FT processor with radiation tolerance to all radiation effects of concern in a space environment. Part of the radiation tolerance is achieved with Ramon Chip's RadSafe™ radiation-hard-by-design library: Single Event Latch-up (SEL) immunity; Total Ionizing Dose (TID) immunity up to 300krad(Si); Single Event Upset (SEU) hardening of sequential logic and configuration registers by means of SEU hardened flip-flops; Single Event Transient (SET) hardening of combinatorial logic, clock networks, and Delay-locked-loop (DLL) circuits. Remaining hardening of all on-chip SRAM memories is achieved by error correction techniques provided by Aeroflex Gaisler with the fault tolerant version of the LEON3 processor. The radiation hardening concept is similar, but not identical, to the one used for the UT699 LEON3-FT processor provided by Aeroflex Colorado Springs. Radiation test results of UT699 were reported in 2009 [1].

This paper reports radiation test results for TID, SEL, and SEU of the newly developed processor. It also reports on the soft error protection concept implemented in processor. Single event upset testing is performed with application tests representing a worst-case scenario for actual application cases in a space environment.

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II. Experimental Details

A. Product Description

The tested GR712RC device is a pipelined monolithic, high-performance, fault tolerant 32-bit SPARC™ V8 LEON3-FT dual core processor [2], [3]. A compliant 2.0 AMBA bus interface integrates the two on-chip LEON3-FT processor cores with a memory controller, a 192 kbyte on-chip RAM memory with EDAC, two RMAP SpaceWire ports, programmable interrupt peripherals, a timer unit with four timers including watchdog, and a switch matrix for additional interfacing of among others Ethernet, four additional SpaceWire ports, six UARTs, CCSDS TM/TC, Mil-Std-1553B, two CAN controllers, general purpose I/Os, SPI, and I2C. Fig. 1 is showing a functional block diagram of GR712RC. The GR712RC is SPARC V8 compliant; compilers and kernels for SPARC V8 can therefore be used as industry standard development tools.

The device is powered with a nominal 3.3V I/O and 1.8V core voltage. 100% load of both processors results in power consumption of 1.5 Watt operating at 100 MHz clock frequency. The device operates at 100 MHz from -55°C to +125°C.

B. Soft Error Protection Concept

The LEON3-FT fault-tolerance features are designed to detect and correct SEU errors in on-chip SRAM memories. The features can be divided in two categories: cache memory protection and register file protection. The cache memory in GR712RC consists of separate instructions and data caches, each 16 kbyte large. Each cache has two parts; tags and data memory. The tag and data memories are implemented with on-chip SRAM memories and protected with four parity bits per 32-bit word, allowing detection of up to four simultaneous errors per cache word. Upon a detected error, the corresponding cache line is flushed and the instruction is restarted. This operation takes 6 clock cycles and is transparent to software.

The processor's Integer Unit (IU) register file is implemented with on-chip SRAM memories. It is protected using Bose-Chaudhuri-Hocquenghem (BCH) coding [4] capable of correcting one error and detecting two errors (SEC/DED) using seven check-bits per 32-bit word. The error detection and corrections has no impact on normal operation, but the correction will delay the current instruction by 6 clock cycles. An uncorrectable error in the IU register file will generate a register-file error-trap.

For either cache or IU register file memory, error checking is performed during memory reads and is therefore dependent upon the application, clock speed, and memory access rates. For diagnostic purposes, error counters are provided to monitor detected and corrected errors in both the IU register file and tag and data parts of the two caches.

The register file of the Floating Point Unit (FPU) is implemented with the hardened flip-flops provided with the RadSafe™ library. No additional error correction of the FPU is implemented.

The all-digital DLLs are protected from SEUs by using hardened flip-flops. The clock network is protected from SETs with dedicated glitch filters.

C. Test System

The test hardware consists of a board hosting one GR712RC device connected to one Flash PROM device, one SRAM device, and one UART RS232 transceiver device. Additional circuits on the board are an oscillator providing the system clock; three power regulators on the board distributing power to the core and I/Os of the GR712RC and the peripheral circuits; and a power management circuit controlling the reset signal to the GR712RC and the memories.

A host computer is connected via the UART interface to the GR712RC. During irradiation, test software is running on the GR712RC reporting its status and results to the host computer running a monitoring software.

The test software is stored in the Flash PROM. At start-up of the processor the software is transferred from the Flash PROM to the SRAM wherefrom the software is executed.

D. Test Software

Two different test programs have been used for SEU testing, "IU-test" and "Paranoia test". While the Device Under Test (DUT) is being irradiated, one of these test programs is executed continuously. In each loop of the test program, a self-checking test task is executed and any test failure is reported to the host computer over the UART channel. Moreover, it reports results and its status to the host: that it is actually running, the value of the internal bit error counters, and the status of the trap registers.

The "IU-test" is a synthetic application designed to access all caches and the IU register file. Each iteration of the test program operates in four steps: a data array with the size of the data cache is allocated and initialized with predefined contents (1), a checksum is calculated by summing the contents of the array (2), the checksum is compared against a pre-calculated value (3), if the result is not equal an IU test failure is reported to the host system (4). Since the allocated data array has the same size as the data cache, all locations of the data cache will be accessed in each iteration. The calculation of the checksum is done with discrete statements rather than a short loop. The code size for the checksum routine is thereby large enough to utilize the full instruction cache in each iteration. To test all registers in the register file, a recursive routine is called once in each iteration. The recursion is 13 levels deep and guarantees that all register windows will be written to memory and then restored again. The "IU-test" program thus achieves near 100% coverage of all on-chip memory during each iteration of the software. Operating at 100 MHz, each iteration takes 3.6 ms. The risk for error build-up during one iteration is thus minimal.

The "Paranoia test" executes the double-precision Paranoia FPU validation test bench [5]. The test bench performs numerous tests to validate the floating-point handling of a processor. All FPU calculations are verified against values calculated in the IU. The program consists mostly of integer instructions; only 5% of the executed instructions are floating-point operations. This makes the program suitable as a combined IU/FPU application. In addition, the program is almost totally self-checking; any undetected errors in the FPU calculations would be detected as an FPU failure by the software cross-checking. Also undetected errors in IU can cause a reported failure as a result of the cross-checking between IU and FPU. In the same manner as in the "IU test" a recursive routine is called before each iteration of the "Paranoia test". Operating at 100 MHz, each iteration takes 6.6 ms.

Both these test programs have earlier been used for SEU testing of the UT699 processor [1], but are here modified to fit the configuration of the GR712RC processor.

E. Single Event Latch-up Testing

Immunity of GR712RC for Single Event Latch-up (SEL) has been verified with heavy ion irradiation tests on two devices. GR712RC was tested under worst-case conditions for latch-up, which is at maximum temperature and voltage. With heating element the DUT was heated to +125°C. The temperature was monitored with a PT100 element attached to the package body. The supply voltages were set to 3.66V and 1.98V for I/O and core, respectively. The SEL testing was performed with the device executing the "IU test". Any event that could cause the DUT to stop operating would manually be recovered by re-initiating the operation of the DUT from the host computer. The system clock frequency was 10 MHz. The core and I/O supply current was continuously monitored for any latch-up event.

F. Single Event Upset Testing

Heavy ion SEU test of the GR712RC was performed executing the "IU test" and "Paranoia test", each in separate test runs. Three different cases for clocking and system frequency have been used: 10 MHz without DLL, 100 MHz

without DLL, and 100 MHz with 2xDLL enabled (50 MHz input frequency). All tests were performed at ambient temperature with supply voltages as in the SEL testing. The temperature on the package body of the device was monitored during all testing, being between +34°C and +46°C. The actual junction temperature varies with the power consumption; which is a function of the clock frequency and the test program.

G. Total Ionizing Dose Testing

Two devices were irradiated with a Cobalt-60 source in one single irradiation step achieving a total ionizing dose of 300 krad(Si). The dose rate was 6.5 krad(Si)/h, namely longer than 46 hours of irradiation. The irradiation session was followed by 168 hours of room temperature annealing and then by 168 hours ageing at +125°C. During irradiation, annealing and ageing, the devices were static biased with nominal supply voltage. Functional test and all DC electrical parameters defined in the datasheet were measured and recorded: before and after irradiation, after annealing, and after ageing. Initial and final electrical measurements were performed at -55°C, +25°C, and +125°C whereas intermediate electrical measurements were performed at +25°C only.

H. Test Facilities

Heavy ion testing was performed at the Heavy Ion Irradiation Facility (HIF) of CYCLONE [6], [7] in Louvain-La-Neuve, Belgium. The M/Q=4 and the M/Q=5 cocktails were used providing LETs ranging from 1.1 MeV-cm^2/mg to 32.6 MeV-cm^2/mg and 3.3 MeV-cm^2/mg to 67.7 MeV-cm^2/mg, respectively.

Total ionizing dose testing was performed with the Cobalt-60 source at Soreq Nuclear Research Center in Israel.

III. Results

A. Total Ionizing Dose

Of all electrical parameters measured after irradiation, annealing and ageing, the only change recorded was a small increase of the standby supply current. Highest current was measured directly after irradiation. After 168 hour of annealing the current returned to 3mA compared to the initial measurement which was below 50µA. After ageing the current returned to the initial value.

B. Heavy Ion Testing

SEL testing up to a fluence of 1×10^7 ions/cm^2 was performed on two devices at highest available LET without recording any latch-up. Tests were performed with normal incident angle and 55° tilting, achieving an effective LET of 67.7 MeV-cm^2/mg and 118 MeV-cm^2/mg, respectively.

SEU testing was performed with the "IU test" and "Paranoia test". Results from "IU test" performed at 100MHz without DLL are presented in Fig. 2. Each test run presented in Fig. 2 was ended after achieving at least 500 detected errors or a total fluence of 1×10^7 ions/cm^2. The flux was kept low ensuring correct error counting, in all test runs the average error rate was below 0.1 errors per test iteration. No IU test failures were recorded.

Results from the "IU test" with different operation cases and from the "Paranoia test" will be presented in the final paper with discussions and conclusions. These tests were performed to a higher fluence in order to better study rare events like system hangs and error traps. The testing was completed 6th of July 2011 not giving time enough to analyze and report all data before deadline for submission of the extended summary. On the 9th July more tests will be performed with the low LET/high penetration cocktail (M/Q=4) provided at HIF. Fig. 2 will be complemented with data with LET down to 1.1 MeV-cm^2/mg.

IV. Discussions

A. Total Ionizing Dose

The TID test demonstrates that the device is capable for 300

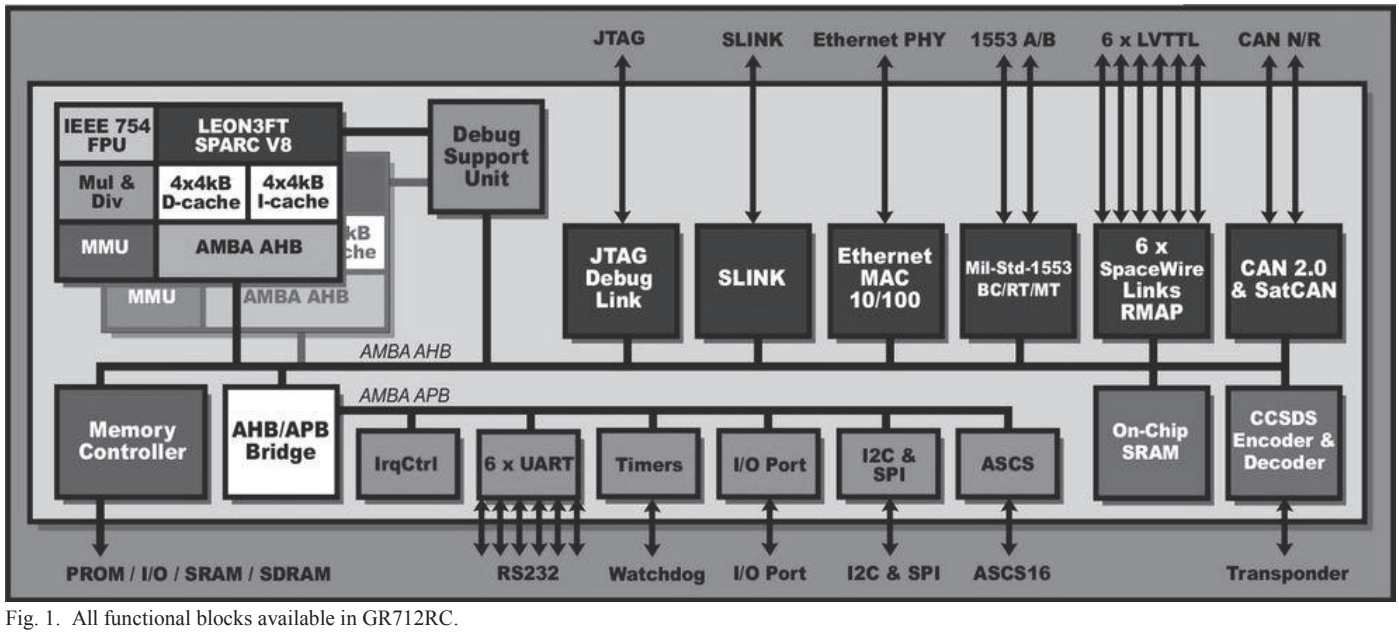

Fig. 1. All functional blocks available in GR712RC.

krad(Si) space environment. The increase of the standby current is marginal and the recovery after ageing demonstrates that no rebound effects exist. Thereby, it can be assumed that the measurement of 3mA after 168 hour of annealing represent the worst case current increase in a space environment where the dose rate is many order of magnitudes lower than the one used in the TID test.

B. Single Event Upset characteristics of SRAM elements

The error statics gathered in heavy ion test in Fig. 2 can be correlated to the actual upset cross section of the underlying SRAM elements by comparing the results with simulated SEU testing by means error injection. While running the test programs under same conditions as in heavy ion test, errors was randomly injected into the cache data and IU register file via the debug interface of the GR712RC. The error counting of the test program ("Effective Errors") is compared to the statistics of injected errors in Table I for the "IU test". In the final paper the error statistics per module from heavy ion test will be compared with error injection statistics.

The SRAM bit cross section can be estimated by dividing measured error cross section in heavy ion test with the detection ratio determined with error injection and dividing with the total number of bits. For the "IU test", the detection ratio is 69.7%. The total number of SRAM bits, including check bits, in the cache memoires and IU register file is 432,128. Hence the measured saturation cross section of the "IU test" of 6.6×10^{-3}cm^2/device (Fig. 2) corresponds to a SRAM bit saturation cross section 1.6×10^{-8} cm^2/bit. The result correlates well with earlier SEU test data on SRAM test structures performed on a test chip for the RadSafe™ library [8], especially at lower LETs. At higher LETs the measured cross section on the test structures is three times higher. This could be an effect different supply voltages (1.8V/3.3V versus 1.98V/3.66V) and multi bit upsets from single ion strikes at higher LETs. The error counters in GR712RC can report up to four multi bit errors as a single error.

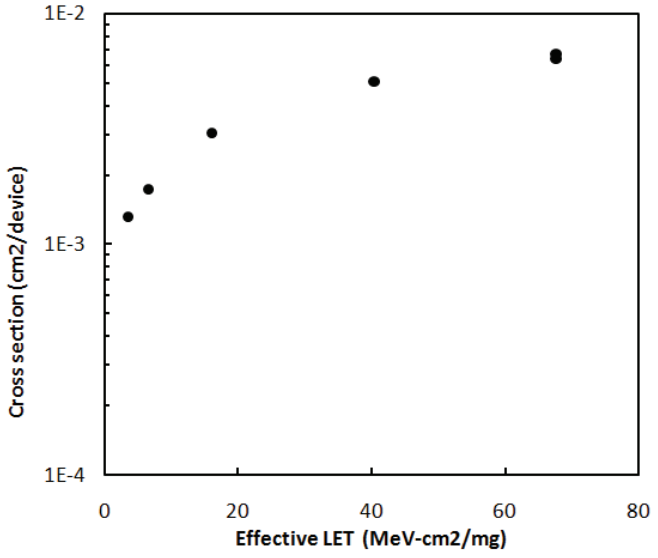

Fig. 2. Error cross section as a function of effective LET for the correctable errors in the "IU test".

TABLE I
RESULTS OF ERROR INJECTION WITH "IU TEST"

Module	Injected Errors	Effective Errors	Ratio Effective/Injected
Instruction cache tags	1,187	1,171	98.7%
Instruction cache data	8,432	4,287	50.8%
Data cache tags	2,263	2,238	98.9%
Data cache data	8,784	7,072	80.5%
IU Register File	638	208	32.6%
Total	***21,522***	***14,976***	***69.6%***

System frequency was 100 MHz with in average 0.5 errors per second injected randomly for twelve hours.

The results of the "IU test" have demonstrated the effectiveness to correct all errors from single ion strikes with no error build-up jeopardizing the error protection. In theory, multi ion strikes in one word before any previous errors in the same word have been corrected could jeopardize the error protections. However, the probability for this to occur in a space environment is negligible thanks to the low flux and continuously accessing of the cache and register file achieved with normal usage of the processor. The actual probability for multi bit errors per word can be calculated: with SRAM SEU cross section data presented in this work, the intended orbit of the spacecraft, and the maximum time between accesses of cache and register file for the specific application case. In the final paper probability for multi bit errors in an example application case will be presented for a geosynchronous orbit.

V. CONCLUSION

Results from TID test, SEL test, and SEU test demonstrates the suitability for operating GR712RC in a space environment. Results from the high fluence SEU tests and SEU test with the low LET/high penetration cocktail remains to be analyzed. It will be reported in the final paper.

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