SUPPLY VOLTAGE AND TEMPERATURE VARIATIONS IN SYNCHRONIZATION CIRCUITS

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***Abstract*— Synchronizers play a key role in multi-clock domains systems on chip and their performance is usually measured by the MTBF of the system. Recent synchronizer metastability measurements indicate degradation of MTBF with technology scaling of circuits in 65nm and below. This degradation of parameters becomes critical when the system is operated at extreme supply voltage and temperature conditions. In this work we study the behavior of synchronizers in a broad range of supply voltage and temperature conditions. A new model for the metastability time constant (τ), the metastability window (T_W) and MTBF is presented. We show a detailed comparison of model, measurements and simulations for different technology nodes and discuss implications for modern synchronization systems. We propose design guidelines that account for supply voltage and temperature variations and determine the correct number of synchronizer stages required for target MTBF.**

***Index Terms*— Measurement method, metastability, MTBF, resolution time constant, synchronization, synchronizer, supply voltage dependence, temperature dependence.**

I. INTRODUCTION

MULTIPLE-CLOCK SYSTEM ON CHIP (SOC) designs require synchronization when transferring signals and data among different clock domains and when receiving asynchronous inputs. Such synchronizations are susceptible to metastability effects [1], which may cause malfunction. To mitigate the effects associated with metastability, latches and flip-flops are often used to synchronize the data [2]. However, there is still a certain probability that the circuit will not resolve its metastable state correctly within the allowed time. To enable assessing the risk, and to design reliable synchronizers, models describing the failure mechanisms for latches and flip flops have been developed [1][2][3]. Most models express the risk of not resolving metastability in terms of the mean time between failures ($MTBF$) of the circuit (1),

$$MTBF = \frac{e^{S/\tau}}{T_W \times F_C \times F_D} \qquad (1)$$

where F_C and F_D are the clock and data transition frequencies, S is a pre-determined time allowed for metastability resolution, τ is the resolution time constant, and T_W is a parameter describing a vulnerable time window which is determined experimentally. T_W and τ are device and technology dependent.

Desirable values of $MTBF$ depend on the application and range from several years upwards. Usually the synchronizer design phase consists of determining the number of stages that would lead to a specified $MTBF$ for a given technology, circuit library and operating conditions.

Recent measurements and simulations [4] [5] [6] [8], indicate that supply voltage and temperature variations highly affect metastability parameters, raising the need for full characterization at different operating conditions. For digital systems that are at risk of metastability failures, the risk of metastability failures may be higher in extreme PVT corners. Synchronizer parameters τ and T_W in (1) can be seen as depending on supply voltage and temperature: $\tau(V_{DD}, T), T_W(V_{DD}, T)$. As a result, careful simulation of the system design at several points throughout its operating region, combined with verification, is proposed as a dependable approach to the detection of potential metastability failures. However, to discern the contribution of each parameter, we seek a formula that calculates $MTBF$ for arbitrary combinations of V_{DD}, T, and is based on semi-empirical parameters determined by measurements or simulations.

In this paper we introduce an analytical model that is able to predict τ, T_W and $MTBF$ with high accuracy. We provide a thorough study of the effect of supply voltage and temperature variations, and present an overall analysis, showing measurements, simulations and model.

The paper is organized as follows. In Section II we review previous published work on temperature and supply voltage influence on metastability parameters. A model describing τ, T_W, and $MTBF$ under temperature and supply voltage variations is presented in section III. Section IV shows the model results and comparisons to measurements and simulations. Section V presents different bounds for T_W and discusses synchronizer design considerations and common errors in calculating the number of synchronizer stages. Section VI summarizes the work.

II. RELATED WORK

The dependence of metastability parameters on temperature and supply voltage has been studied in the literature by means of simulations and measurements. Table I summarizes relevant work in metastability measurements and simulation results under varying V_{DD}, T and process technology. The first part of the table considers reported metastability measurements. Those measurements are performed using a wide range of methods, devices (off the shelf components, SoCs, FPGA, etc.), and diverse technology nodes. The *Simulations* section of the table represents simulation only results, without measurements to

validate dependence on variations. The *Measurements vs. simulations* section includes publications comparing simulations to measurements for actual circuits. Rows in the table indicate different process technology or circuit.

Most publications provide measurements or simulations for a specific circuit under nominal supply voltage and temperature conditions. In [5] a comparison of simulations and measurements for varying supply voltage and temperature is performed. While the publications listed in Table I shed light on the dependence of metastability parameters on supply voltage and temperature, this paper combines a theoretical analysis with an exhaustive comparison between simulations and measurements over the entire relevant range. To the best our knowledge, such model and analysis has not been proposed yet.

TABLE I
SUMMARY OF EXISTING METASTABILITY MEASUREMENTS/SIMULATIONS RESULTS

CATEGORY	EXISTING WORK
Metastability measurements	[11],[12] – First metastability measurements, nominal V_{dd} and T. [13] –Non-constant τ measuremnt, nominal V_{dd} and T. [14], [15], [19], [22], [23]– Various circuits measurements, nominal V_{dd} and T. [17] – 2µm and 1,2 µm technology nodes measurements for different V_{dd} nominal T. [16] – 1.5 µm and 1.0 µm for different V_{dd}, T. [3]– 0.25 µm CMOS, nominal V_{dd} and T. [18], [20] – Programmable logic device (PLD), nominal V_{dd} and T. [6], [8],[9],[26]– 90nm CMOS FPGA, different V_{dd} nominal T [10] –Different FFs in 65nmCMOS, nominal V_{dd} and T. [27] – 40nm CMOS, nominal V_{dd} and T.
Metastability Simulations	[7] –0.35µm, 0.25 µm and 0.18 µm technology nodes, nominal V_{dd} and T. [21] – 0.18 µm CMOS, different V_{dd} and T. [24] – 65nm CMOS for different FF's and V_{dd}, nominal T. [25] –90nm[a] CMOS, different V_{dd} and body bias, nominal T.
Measurements vs. simulations	[5] – 0.18 µm[b] for different V_{dd}, nominal T. [4] – 0.65 µm[b] for different V_{dd}, nominal T.

[a] On-chip measurement method
[b] Process variability study.

III. MODEL

To quantify the effect of temperature and supply voltage variations on τ, T_w and $MTBF$, we seek a semi-empirical formula that is able to provide insights of the physical effects influencing τ, T_w and $MTBF$, while also being sufficiently simple in order to alleviate the need for numerous simulations at different (T, V_{dd}) combinations.

We consider a generalized flip-flop circuit, similar to the one shown in Figure 1. The circuit comprises a master and a slave latch. Each latch is characterized by a resolution time constant τ_i $(i \in \{m, s\})$. We start our analysis presenting a semi empirical model for τ_i, and continue to develop an empirical model for T_W. We then combine the models for τ and T_W using (1) to derive a semi empirical model for $MTBF$.

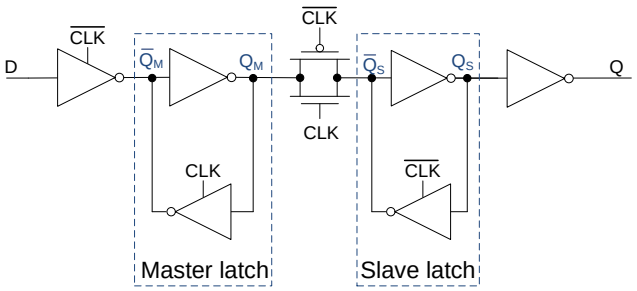

Figure 1. Master-slave circuit

A. τ Model

Based on the resolution time constant for each latch in a flip-flop, the overall effective resolution time constant for the flip-flop is given by [28]

$$\tau_{eff} = \left(\frac{\alpha}{\tau_M} + \frac{(1-\alpha)}{\tau_S}\right)^{-1} \tag{2}$$

where α represents the duty cycle of the clock. Using this formula, a model for the resolution time constant of each latch can be obtained and then joined using (2).

Based on small signal analysis, τ can be approximated by [13]:

$$\tau \propto \frac{C_Q}{g_m} \tag{3}$$

where C_Q includes the gate and diffusion capacitance of the metastable synchronizer nodes $(Q_i, \bar{Q}_i, i \in (m, s))$ and the coupling capacitance between the gate and the source and drain of the transistors connected to the metastable nodes. g_m is the transconductance of the transitors in the latch. Figure 2 shows a standard library flip-flop circuit. The master and slave latches are marked by dashed lines. For the master latch C_Q includes the gate capacitances of inverter INV1, T5, T8 and INV2 and the diffusion capacitances of transistors T6,T7,T2,T3 and INV1. For g_m of the master, the transistors involved in the transconductance are T5,T6,T7,T8 and INV1.

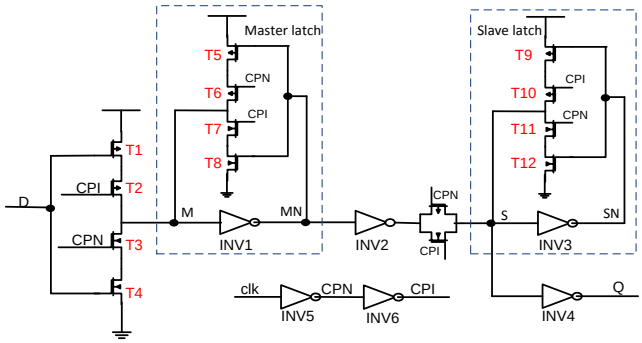

Figure 2. Library flip-flop circuit.

Near metastability, the transistors operate in the linear region, and hence the transconductance can be approximated by:

$$g_m = g_{mn} + g_{mp} = \tag{4}$$

$$\left(\mu_n C_{ox}\frac{W_n}{L}\frac{1}{1+\sqrt{a}}+\mu_p C_{ox}\frac{W_p}{L}\frac{\sqrt{a}}{1+\sqrt{a}}\right)(V_{DD}-|V_{ThP}|-V_{ThN})^{\alpha}$$

where $a=\mu_n W_n/\mu_p W_p$, V_{TN} and V_{TP} are the transistor threshold voltage for the *N* and *P* transistors, respectivelly, μ_n and μ_p are the electron and hole mobilities and α is the velocity saturation index, whose typical value is around 1.3 [29].

The mobility dependence on temperature can be approximated by [30][31]:

$$\mu = \mu_0\left(\frac{T_0}{T}\right)^{\alpha_\mu} \tag{5}$$

where T is the temperature, T_0 is the nominal temperature, μ_0 is the mobility at T_0 and α_μ is an empirical parameter referred to as the mobility temperature exponent, usually around 1.5. In a similar way, the threshold voltage dependence is given by:

$$V_{Th}(T) = V_{Th0} + \alpha_{VTh}(T - T_0) \tag{6}$$

where V_{Th0} is the threshold voltage at T_0, and α_{VTh} is the threshold voltage temperature coefficient, a negative coefficient with typical values around –2 mV/K [31]. Note that the *drain-induced-barrier-lowering* (DIBL) effect [32] has been neglected since in metastability the voltage at the drain is around $V_{DD}/2$.

Combining (3),(4),(5) and (6) for *N* and *P* type transistors the following proportionality is derived:

$$\tau \propto \frac{T^{\alpha_\mu}}{(V_{DD}-(V_{ThN0}+\alpha_{VThN}(T-T_0)-|V_{ThP0}+\alpha_{VThP}(T-T_0)|))^{\alpha}} \tag{7}$$

Based on (7) we can derive the following semi-empirical formula for (T, V_{DD}) dependence of τ:

$$\tau(T, V_{DD}) = \frac{A\cdot T^{\alpha_\mu}}{(V_{DD}-(2V_{ThE}+\alpha_{VThE}(T-T_0)))^{\alpha}} \tag{8}$$

where V_{ThE} is a parameter representing an effective threshold voltage, α_{VThE} an effective voltage temperature coefficient and A is a multiplicative constant with appropriate units.

B. T_W Model

In contrast with the model for τ, we use an empirical model for T_W with respect to (T, V_{DD}). This is because T_W does not constitute an inherent physical constant of the system. Rather, it is a coefficient arising from $MTBF$ modeling [33]. We have chosen a relatively simple model based on trading off accuracy for simplicity, for two reasons. First, since the effect of T_W on $MTBF$ is linear (1), its influence on *MTBF* is significantly smaller compared to the exponential effect of τ. Thus, reducing accuracy in the modeling of T_W will result in a relatively small inaccuracy in $MTBF$. Second, the model employs fitting to T_W values determined by simulations and measurements; these values are noisy, and a low order fitting model is preferred as it avoids over-fitting, effectively low-pass filtering the noise. We validate those assumptions in the following sections, where we present results, and compare values of *MTBF* using different T_W bounds.

Based on measurements and simulations [4], a non-linear model for T_W is proposed:

$$T_W(T, V_{DD}) = \sum_{i,j=1}^{2} a_{i,j}\, x_i\, x_j + \sum_{i=1}^{2} b_i\, x_i + c$$
$$x_1 = T \qquad x_2 = V_{DD} \tag{9}$$

The coefficients $a_{i,j}, b_i\ (i,j \in \{1,2\})$ and c are determined by a non-linear least square procedure. The constants $a_{1,2}$ and $a_{2,1}$ are both coefficients of square terms of the form TV_{DD} and are grouped in a single coefficient named $\tilde{a}_{1,2}$. Overall for the T_W model, we are left with 6 parameters: $a_{1,1}, a_{2,2}, \tilde{a}_{1,2}, b_1, b_2, c$.

C. MTBF Model

To express the $MTBF$ dependence on T and V_{DD}, we combine (1) ,(8) and (9) to obtain:

$$MTBF(T, V_{DD}) = \frac{\exp\left(\frac{S}{A\cdot T^{\alpha_\mu}(V_{DD}-(2V_{ThE}+\alpha_{VThE}(T-T_0)))^{-\alpha}}\right)}{\left(\sum_{i,j=1}^{2} a_{i,j}\, x_i\, x_j + \sum_{i=1}^{2} b_i\, x_i + c\right)\times F_C \times F_D} \tag{10}$$

We define two useful parameters, the temperature coefficient of $MTBF$ (TCM) and the supply voltage coefficient of $MTBF$ (VCM). TCM expresses the relative change of $MTBF$ when the temperature is changed by one degree Kelvin. The VCM is the analogous form for supply voltage change of 1V. TCM and VCM estimations can be obtained from (10):

$$TCM \triangleq \frac{1}{MTBF}\frac{dMTBF}{dT} = -\frac{S}{\tau}\left(\frac{1}{\tau}\frac{d\tau}{dT}\right) - \left(\frac{1}{T_W}\frac{dT_W}{dT}\right) \tag{11}$$

In a similar way:

$$VCM \triangleq \frac{1}{MTBF}\frac{dMTBF}{dV_{DD}} = -\frac{S}{\tau}\left(\frac{1}{\tau}\frac{d\tau}{dV_{DD}}\right) - \left(\frac{1}{T_W}\frac{dT_W}{dV_{DD}}\right) \tag{12}$$

The expressions in parentheses in (11) and (12) are the relative change in τ multiplied by the factor $\frac{S}{\tau}$, and the relative change in T_W when T or V_{DD} are increased by one degree or by one volt, respectively.

IV. Model Evaluation

In order to evalute the validity of the proposed model we compare it with measurments and simulations (which were described in [4]). A synopsys of measurements and simulation results are given, followed by comparing them to model results, and by analyzing the sensitivity of the model to TCM and VCM parameters.

A. *Simulations and measurements results*

Figure 3 compares τ simulations and measurements for a 65nm LP CMOS library master-slave flip-flop (Figure 2) used as a synchronizer. The measurements have been performed in pre-selected typical/typical (TT) parts, and represent an average of eight measured chips. Simulations used for comparison were carried out using the method described in [34][35], which sweeps clock and data signals to predict τ and T_W values.

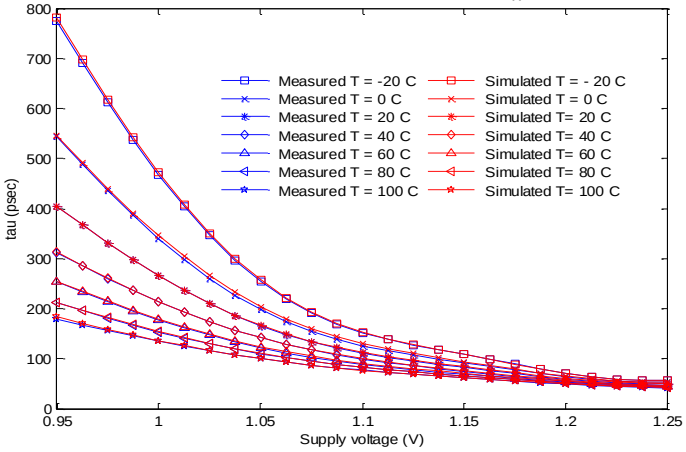

Figure 3. τ Measurements and simulation results versus supply voltage for different temperatures.

The difference between τ measurements and simulations is less than 3.2% over the entire set of supply voltage and temperature combinations. As described in [4], this difference is consistent with the measurement error in τ, estimated at 5%.

Figure 4 shows T_W measured and simulated results versus temperature for different supply voltages. Simulated values show an oscillatory trend due to simulation dependence upon initial conditions and integration error. Measured values of T_W are highly affected by absolute errors in the delay measurements [4]. Due to high process variations in deep sub-micron technologies, the delay for some gates can differ greatly from the mean delay of identical gates in the circuit. Those variations may reach 40% in 65nm [36], and affect T_W measurements as shown in [4]. In section V we evaluate the error incurred by using different T_W bounds, and their impact on $MTBF$.

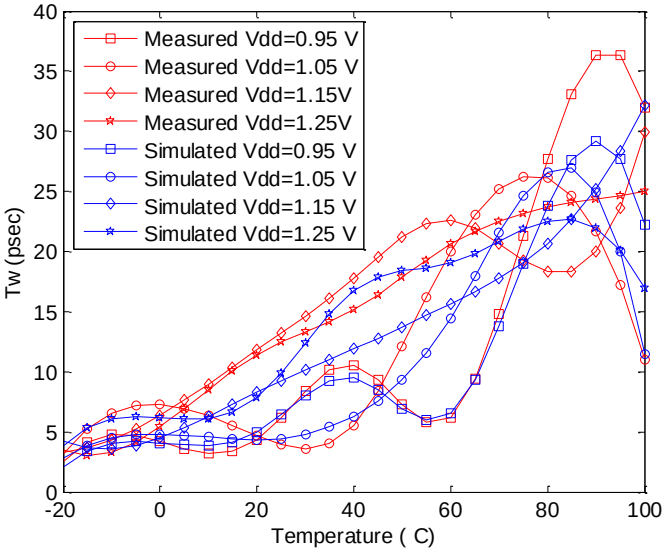

Figure 4. τ Measured and simulated results versus temperature for different supply voltages.

B. *Model results*

In this sub-section we compare the model derived in section III to measured and simulated values, and calculate the accuracy of the model for different technologies.

Figure 5 shows a comparison of model (8) (solid surface) and measured values for τ (dots). Figure 6 and Figure 7 show voltage and temperature cross sections of Figure 5. The empirical model parameters were obtained by means of a trust-region non-linear least square approximation [37],[38] of the measured values with respect to (8), as shown in Table II. The goodness of fit is given by the coefficient of determination (R-square) and the adjusted R-square. Both are needed in order to avoid a scenario of *Anscombe's quartet* [39], where an R-square value close to unity doesn't guarantee a good fit because of model over fitting. In our case, both R-square and the adjusted R-square values are close to unity, indicating a good fit of the model to measurements. In addition, Figure 6 and Figure 7 show that there are no outliers in the data set. The root mean square error (RMSE) of the fit determines that the average error induced in using the model compared to measurements is under 2% in average. Since measurements were shown to follow simulations within less than 5% error (in sub-section A above), simulations can be used with confidence in order to determine model parameters as well. When the supply voltage is high, the temperature influence on τ is reduced (bottom plot of Figure 6), while for lower supply voltage values, a change in temperature may lead to large changes in τ (top plot of Figure 6). Supply voltage though, increases τ significantly for every temperature in the range −20°C to 100°C, the influence becomes larger when the temperature is low (Figure 7).

In general, at least five sets of readings $\{(T_i, V_{DD\,i}, \tau_i)\}_{i=1,..,5}$ are needed to estimate the five model parameters ($A, \alpha, \alpha_{VThE}, \alpha_\mu, V_{ThE}$). Those sets are likely to be obtained by simulations or measurements.

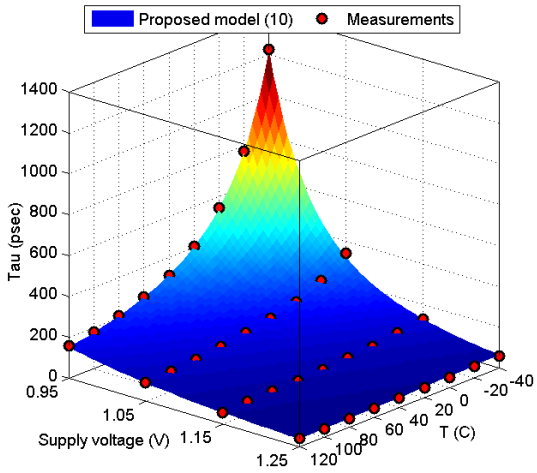

Figure 5. τ analytic model vs measurements results

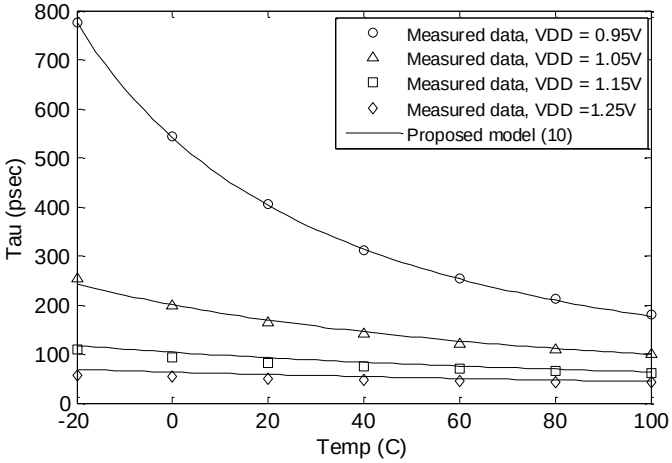

Figure 6. Measurements vs. analytical model, temperature cross sections of Figure 5.

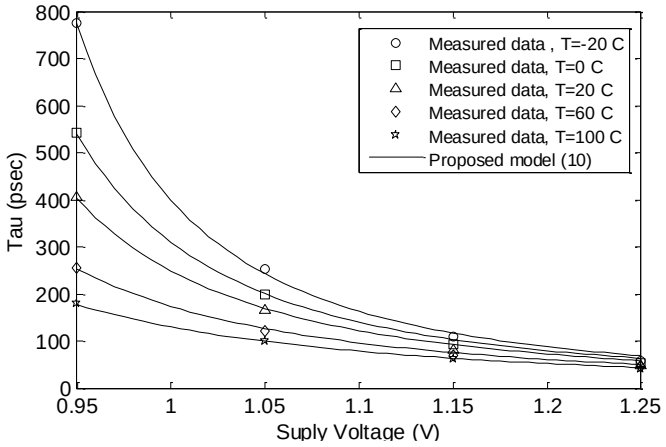

Figure 7. Measurements vs. analytical model, supply voltage , cross sections of Figure 5.

TABLE II
NON-LINEAR LEAST SQUARE FIT OF τ MEASUREMENTS

PARAMETERS	VALUE	UNITS
A	0.00068	
α_μ	1.7	
$2V_{ThE}$	0.784	[V] [a]
α_{VThE}	1.9	[mV/K] [a]
T_0	233	[K] [a]
α	2.8	
RMSE	2.93	psec
$R - sqaure$	0.9996	
Adjusted R - square	0.9993	

[a]V = volt, K=degree kelvin.

Figure 8 shows a comparison of T_W model (9) and simulations. In this case the model represents the trend of T_W for different (T, V_{DD}) as the simulated (or measured) data is noisy. Modeling T_W as a higher order polynomial would produce over fitting to noise data and will not generate reliable values. Table III shows the estimated coefficients of the non-linear least square fit of the simulated T_W to (9). The R-square indicator is significantly lower than 1 (around 0.85), however this ends up in only a small deviation of the $MTBF$ as is demonstrated in the following sub-section. Values of the RMSE demonstrate that the average deviation remains small compared to absolute T_W values. Temperature cross sections of the T_W model for different supply voltages are shown in Figure 9.

T_W increases with temperature approximating a quadratic function. The parabolic nature of T_W is almost unchanged for different supply voltages, as demonstrated by the near parallel curves in Figure 9. T_W also shows an increase with supply voltage, although that change is much smaller than the change with temperature.

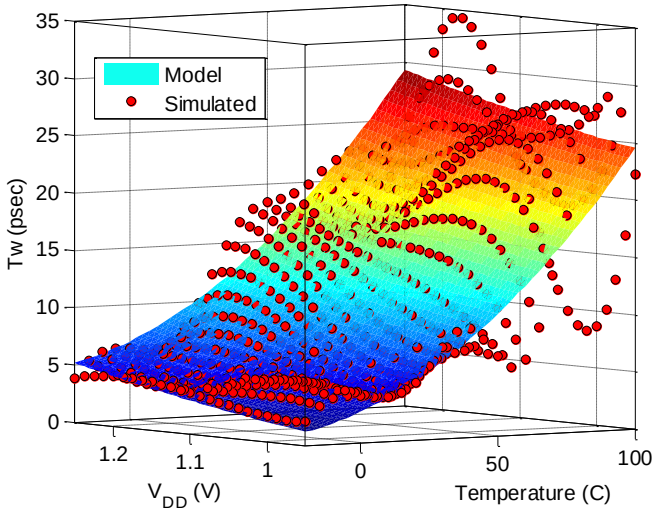

Figure 8. T_W model vs. simulated values

TABLE III
NON-LINEAR LEAST SQUARE FIT OF T_W SIMULATIONS

PARAMETERS	VALUE	UNITS
$a_{2,2}$	0.0954	psec V^{-2} [a]
$\tilde{a}_{1,2}$	0.0762	psec K^{-1} V^{-1} [a]
$a_{1,1}$	1.541	psec K^{-2} [a]
b_1	7.146	psec K^{-1}
b_2	1.33	psec V^{-1}
c	-11.96	psec
RMSE	3.17	psec
$R-sqaure$	0.8455	
Adjusted R-square	0.8442	

[a]V = volt, K=degree kelvin.

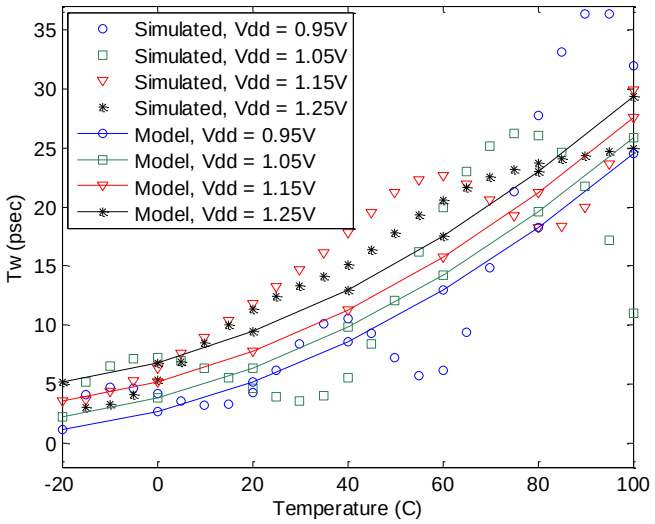

Figure 9. Simulations vs. analytical model, temperature cross section of Figure 8.

Figure 10 shows $MTBF$ model (10) versus simulations. The $MTBF$ corresponds to a clock domain crossing of $f_d = 100Mhz$ and $f_c = 500Mhz$, using a two flip-flop synchronizer. A black plane representing $MTBF$ threshold is also shown, set to 25 years as a representative number. All points with $MTBF$ above the threshold are reliable; points below the threshold are considered unreliable and a circuit operating at that (T, V_{DD}) point is prone to metastability failures. The green surface is the $MTBF$ value calculated using the model while the violet surface is $MTBF$ calculated using simulated values of τ and T_W. The main difference between the surfaces is due to the difference between the T_W model and simulations (rather than to any differences in τ).

Figure 11(a) shows τ temperature sensitivity $\left(\frac{1}{\tau}\frac{d\tau}{dT}\right)$ for different supply voltages. When the supply voltage is higher than the nominal voltage of the technology (1.1V for low power 65nm) τ changes moderately. However, for lower V_{DD} a small temperature change leads to a large percentage change in τ. For $V_{DD} = 0.95V$, $T = 40℃$ an increase of one degree K results in a 1.2% decrease in τ. In the temperature region we studied (−20°C to 100°C) both μ and V_T decrease with increasing temperature [40], however decreasing μ increases τ while decreasing V_{Th} decreases τ. When the impact of a change in μ on τ is larger than the impact of a change in V_{Th} on τ, increasing temperature causes an increase in τ. Conversely, when the impact of V_{Th} dominates over that of μ, increasing temperature causes a decrease in τ. The dominant factor is determined by the value of the supply voltage. In modern technologies, where V_{DD} approaches the value of 2 V_{Th}, small changes in V_{Th} cause larger changes in τ, and it is dominant over μ.

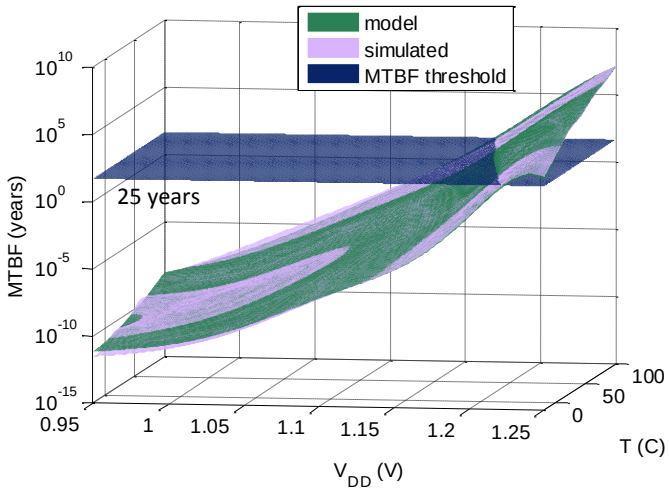

Figure 10. MTBF model vs. simulated results

In addition to showing good match of measurements, simulations and model results on 65nm LP process, the model was tested against τ, T_W simulations for 180nm and 90nm technology nodes. All the results present higher than 0.99 values for R-square and adjusted R-square fit for τ to (8), and higher than 0.85 fit for T_W to (9) as shown in Table IV.

Figure 11(b) presents τ supply voltage sensitivity $\left(\left(\frac{1}{\tau}\frac{d\tau}{dV_{DD}}\right)\right)$ for different temperatures. For high temperatures, V_{Th} decreases and the influence of V_{DD} on τ is smaller. For lower temperatures V_{Th} is larger and when V_{DD} is decreased τ increases by larger margins. In both cases, τ sensitivity to V_{DD} and T, the dependence is negative, meaning, that an increase in V_{DD} or T will induce a decrease in τ. Such analysis is useful, for instance, to specifying the stability of power supplies and power distribution networks on chip. When the amount of noise in the power supply is known, the effect induces a change in τ and a possible decrease in system metastability reliability. This is more significant when IR drops are present, reducing the effective supply voltage seen by the synchronizer circuit and hence increasing τ, which according to (12) reduces $MTBF$.

Analogously Figure 12(a) shows temperature sensitivity $\left(\frac{1}{T_W}\frac{dT_W}{dT}\right)$ of T_W for different supply voltages. Sensitivity increases for lower supply voltages. In Figure 12(b) supply voltage sensitivity $\left(\frac{1}{T_W}\frac{dT_W}{dV_{DD}}\right)$ of T_W is shown. For nominal and high temperatures the sensitivity is almost constant and around 0.2%/V. For lower temperatures the sensitivity increases but still remains lower than 1%/V. Consequently T_W is less sensitive to supply voltage variations than to temperature variations.

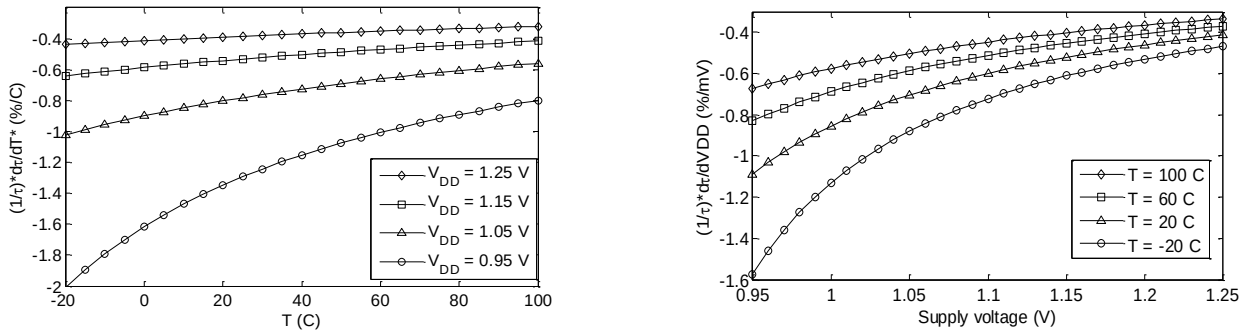

Figure 11. (a) $\boldsymbol{\tau}$ temperature sensitivity $\left(\frac{1}{\tau}\frac{d\tau}{dT}\right)$ (b) $\boldsymbol{\tau}$ supply voltage sensitivity $\left(\frac{1}{\tau}\frac{d\tau}{dV_{DD}}\right)$

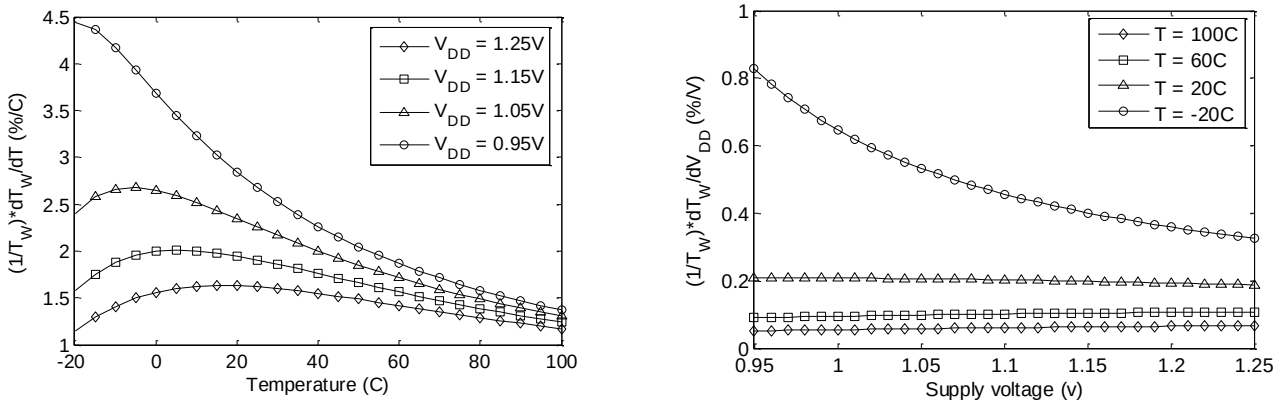

Figure 12. (a) $\boldsymbol{T_W}$ temperature sensitivity $\left(\frac{1}{T_W}\frac{dT_W}{dT}\right)$ (b) $\boldsymbol{T_W}$ supply voltage sensitivity $\left(\frac{1}{T_W}\frac{dT_W}{dV_{DD}}\right)$

TABLE IV
NON-LINEAR LEAST SQUARE FIT RESULTS FOR DIFFERENT TECHNOLOGY NODES

PROCESS NODE	τ		T_W	
	R- SQUARED	ADJUSTED R-SQUARED	R- SQUARED	ADJUSTED R-SQUARED
180nm[a]	0.999	0.998	0.8113	0.8091
90nm[b]	0.9991	0.998	0.832	0.8319
65nm[a]	0.9996	0.9993	0.8455	0.8442

[a]Low power (LP), [b]General purpose (GP)

C. TCM and VCM results

Figure 13 shows TCM curves versus temperature for $V_{DD} = 1.1V$. The graph shows the different components of TCM as in (11). The resolution time (S), which is determined by the frequency of the receiving domain and the number of FFs in the synchronizer, is assumed ten times τ in Figure 13. The trend of TCM is mainly affected by the τ sensitivity and is slightly reduced by the T_W sensitivity. For instance, when the circuit is operated at room temperature (27°C), an increase of one degree in temperature generates a reduction of 1.4% in τ, an increase of almost 1.8% in T_W, and an overall 6% increase in $MTBF$ (assuming $S = 10\tau$).

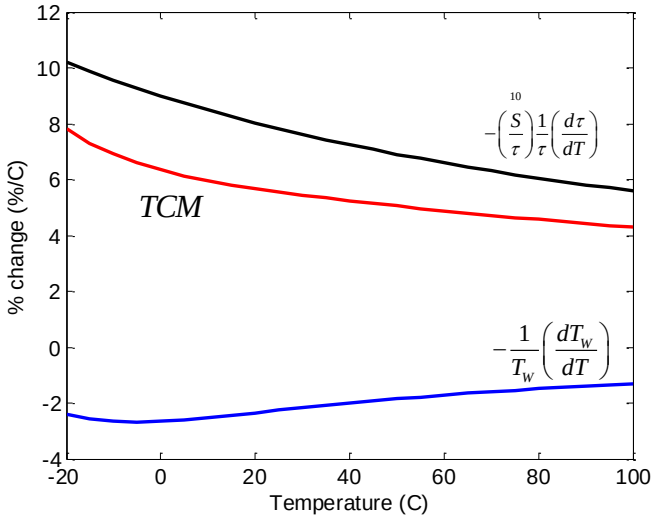

Figure 13. TCM vs. temperature ($\boldsymbol{V_{DD}}$ = 1.1V)

The absolute percentage change in $MTBF$ is determined by the (T, V_{DD}) operating point, and by S, the amount of resolution time. Figure 14 shows TCM versus normalized resolution time for three different corners: Low supply voltage, low temperature corner (LL), nominal voltage, nominal temperature (NN) and high voltage, high temperature (HH). In all cases, TCM increases as resolution time increases, following the linear equation described in (11). When the system is operated near

the LL corner, small S changes generate higher percentage $MTBF$ fluctuations.

It should be noted, that the corner case LL corresponds to a low voltage, *low* temperature case as opposed to delay corners when the slowest circuits appear for low voltage and *high* temperature. In a similar way, the HH case correspond to a high voltage, *high* temperature, while for delay, it is obtained for high voltage and *low* temperature.

Analogous plots for VCM are shown in Figure 15 and Figure 16.

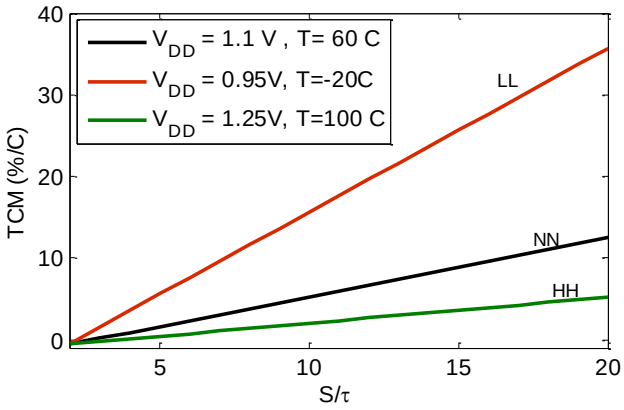

Figure 14 TCM vs. resolution time for different $(\boldsymbol{T}, \boldsymbol{V_{DD}})$ corners.

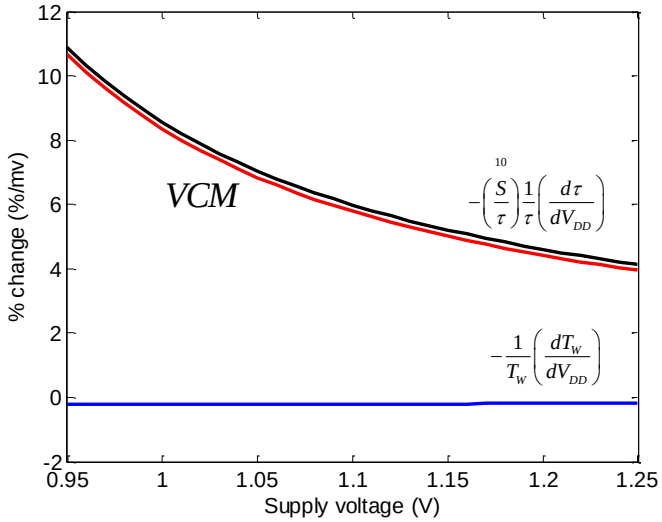

Figure 15. VCM vs. temperature ($\boldsymbol{T}$ = 40°C)

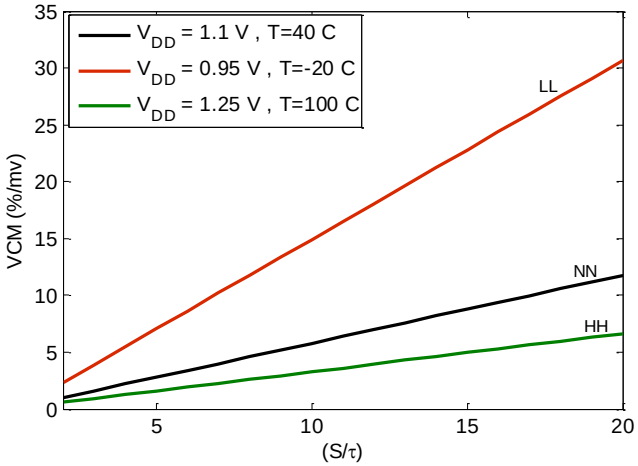

Figure 16. VCM vs. resolution time for different $(\boldsymbol{T}, \boldsymbol{V_{DD}})$ corners.

V. Model Implications

In this section we study the effect of using different bounds for T_W and their impact on the $MTBF$. We also analyze the effects of using those bounds from the perspective of the $VLSI$ designer who is to calculate the number of flip-flops to use in a synchronizer. We finish by presenting useful guidelines to the designer to account for corner (T, V_{DD}) conditions.

A. T_W Bounds

So far, we have developed a model for $MTBF$ based on models for τ and T_W. The τ model was shown to predict simulation and measurement values with minimal error, while T_W model demonstrates a higher error due to the noisy nature of measurements and simulations that were used to fit into the model. In this section we analyze the effect that the T_W model has on $MTBF$ and the number of flip-flops to use in a synchronizer. We study different bounds that compromise accuracy for simplicity.

We compare simulated $MTBF$ values, model calculated values (10), and two bounds named T_{Wmax} and T_{WTc}. T_{Wmax} is the maximum T_W over all (T, V_{DD}) combinations, and T_{WTc} is the clock period, as clearly $T_W \leq 1/f_c = T_C$.

Figure 17 shows $MTBF$ results of simulations, model, T_{Wmax} and T_{WTc} bounds for a system with $f_d = 100MHZ$, $f_c = 300MHZ$ and a resolution time of one clock cycle, meaning a two flip-flop synchronizer. We note that the simulated and model results are correlated with a maximum difference of less than 30%, much less than an order of magnitude for the entire range of supply voltage studied. T_{Wmax} represents a lower bound with a maximum difference of one order of magnitude relative to simulated $MTBF$ values. The T_{WTc} bound provides a less tight lower bound with difference of almost three orders of magnitude below model predictions. The $MTBF$ difference for each of the bounds can be translated to the number of flip-flops to use in a synchronizer to obtain a target $MTBF$ of 25 years. Figure 18 shows the number of flip-flop stages to use when $f_d = 100MHZ$, $f_c = 300MHZ$ and T=27°C. For the nominal supply voltage (1.1V), model and simulations indicate that a two flip-flop synchronizer should be used. However, the T_{WTc} bound indicates a three flip-flop synchronizer incurring an extra

delay of one clock cycle. The difference of the number of stages calculated using the different bounds represents the overprovisioning of each bound. It is clearly noted that the minimum overprovisioning is obtained by the developed model, which for lower supply voltages almost overlaps simulations.

Figure 19 shows results of $MTBF$ versus temperature for the same system as above. The model derived is still closely related to simulations with differences of less than 30% over the studied temperature range, while the bounds present much larger deviations from both simulations and model of one and three orders of magnitude, respectively. It is worth noting that both bounds present higher differences for lower temperatures and supply voltages, which as noted above are the worst cases with respect to metastability resolution.

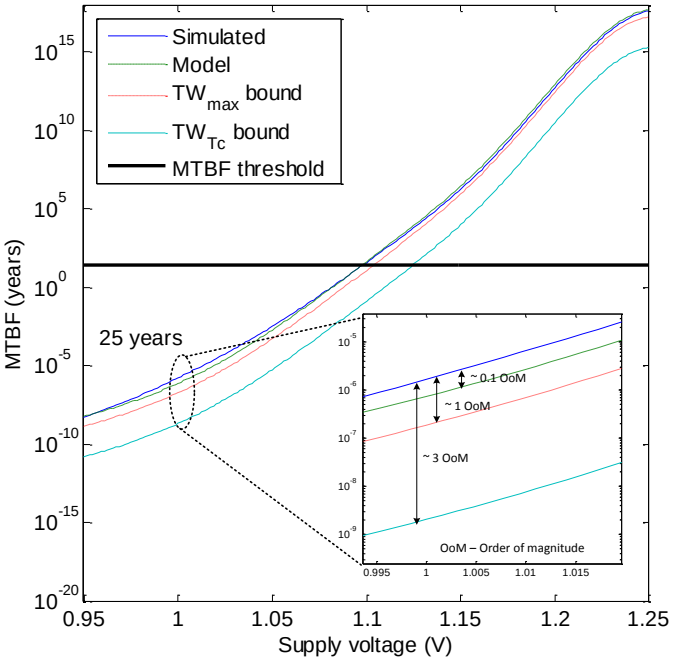

Figure 17. *MTBF* vs. supply voltage for $f_d = 100MHZ$, $f_c = 300MHZ$, using simulations, model and bounds for T_W.

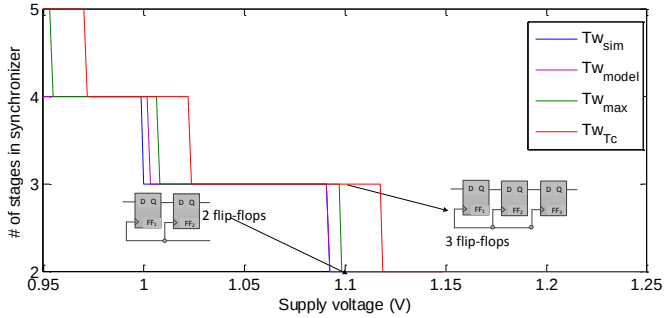

Figure 18. Number of stages in synchronizer vs. supply voltage, using different T_W bounds.

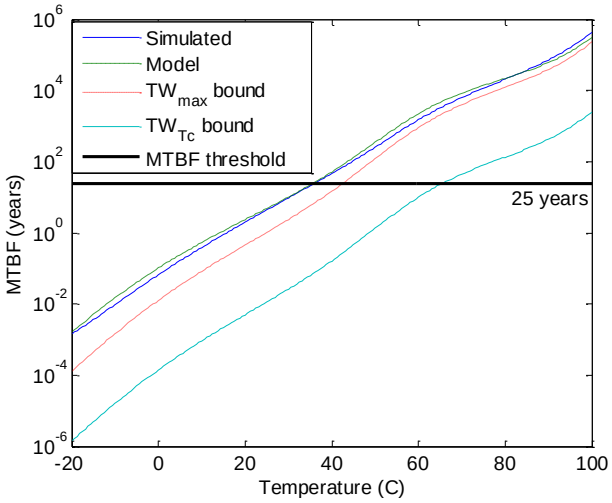

Figure 19. MTBF vs. temperature for a $f_d = 100MHZ$, $f_c = 300MHZ$, using different T_W bounds.

B. Synchronizer design considerations

In this section, we study the model implications from the perspective of the VLSI designer who needs to determine the number of stages to use in a synchronizer, based on the system parameters, the sender and receiver frequencies (f_d, f_c), the technology node and flip-flop libraries which determine τ and T_W, and the reliability of the intended system, as measured by $MTBF$. The usual approach to this task is to estimate the amount of resolution time needed in order to obtain a certain $MTBF$ using (1), followed by the calculation of the number of flip-flop stages to achieve that resolution time. Usually a spare number is always added to account for variations. This spare number can be added to the target $MTBF$ or to the calculated number of stages, but is usually determined by rules of thumb, rather than by quantitative calculations, possibly yielding loose bounds with significant performance loss or underestimations resulting in metastability errors. In this section we identify design guidelines that provide tighter bounds to $MTBF$ and hence alleviate the need of un-necessary flip-flop stages.

To understand the implications of the measurements and model results, we consider synchronization scenarios and calculate the number of stages to be used to achieve a desired reliability. This calculation is based on the model (10), the desired $MTBF$ and the assumption that each additional stage adds a clock period to the settling time S in (1), as proposed in [33]. Model parameters are obtained from previous measurements of a 65nm LP process and standard digital library flip-flops (Table II, Table III). It is also assumed that both master and slave latches in the prospective flip-flops have the same τ and T_W, a usually optimistic assumption [28], but is assumed here for the ease of calculation. We also omit the setup and propagation delay of each flip-flop.

The first guideline is the need to account for the worst case scenario. As was stated in the previous section (Figure 14, Figure 16) the worst synchronization scenario occurs at the low temperature, low supply voltage corner. Figure 20 shows the number of flip-flop stages needed in a synchronizer in order to

achieve an $MTBF$ of 25 years, for a system with $f_d = 100MHZ$, $f_c = 300MHZ$. The number of flip-flops increases drastically for the worst case corner, incurring a very high latency. It is possible to assume that when a circuit is in functional operation, the self-heat generated raises the junction temperature of internal nodes in the circuits above 0°C; thus, the black line in Figure 20 indicates a 0-degree junction temperature limit, below which actual practical operation is unlikely to be encountered. Even when this 0-degree junction temperature limit is considered, the number of flip-flops in nominal operation mode is very different than in the worst case.

A typical error is to omit the worst (T, V_{DD}) corner analysis, and substitute it by an increased $MTBF$ target to account for T, V_{DD} variations. In other words, calculate the number of stages for the nominal (T, V_{DD}) corner using an increased $MTBF$ target value (i.e. doubled $MTBF$) to account for the (T, V_{DD}) variations.

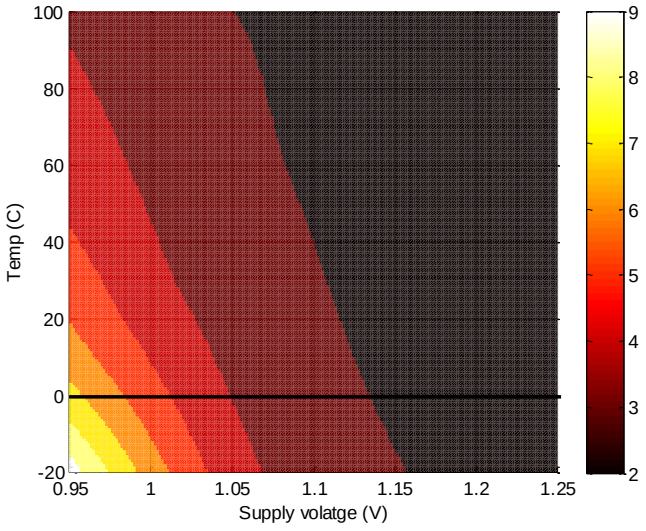

Figure 20. Number of flip-flops in synchronizer for $F_C = 300\ MHz$ and $F_D = 100\ MHz$.

The number of stages (N_S) for a given synchronization is given by (1):

$$N_S = \left\lceil \frac{\tau \cdot ln(MTBF \cdot f_c \cdot f_d \cdot T_W)}{T_C} \right\rceil + 1 \qquad (13)$$

The main difference between the nominal (T, V_{DD}) case and the worst case is reflected by different τ and T_W as shown in Figure 5 and Figure 8. Since τ dominates (Figure 13 and Figure 15), it is the dominant factor in the worst case, where the number of stages is given by:

$$N_S{}^{wc\,(T,V_{DD})} \cong N_S{}^{nom}\left(\frac{\Delta\tau}{\tau} + 1\right) \qquad (14)$$

Where $\Delta\tau$ is the increase in τ for the worst case corner. In the 65nm example, $\frac{\Delta\tau}{\tau} \approx 3$ for the worst case and $N_S{}^{wc\,(T,V_{DD})} \approx 4N_S{}^{nom}$. Then if for the nominal (T, V_{DD}) corner, only two synchronization stages are needed to obtain a desired $MTBF$, in the worst case scenario, the number of flip-flops increases to around 8.

On the other hand, the number of stages needed when an $MTBF$ spare ($\Delta MTBF$) is taken, is given approximately by:

$$N_S{}^{MTBF+\Delta MTBF} \cong N_S{}^{MTBF} + \left\lceil \frac{\tau}{T_C} \frac{\Delta MTBF}{MTBF} \right\rceil \qquad (15)$$

Typically a spare of 50-100% is taken, giving values of $\frac{\Delta MTBF}{MTBF} \approx 1$. Since $\tau < T_C$, this implies that either $N_S{}^{MTBF+\Delta MTBF} \cong N_S{}^{MTBF}$ or $N_S{}^{MTBF+\Delta MTBF} \cong N_S{}^{MTBF} + 1$. This means that doubling the $MTBF$ target adds only one stage to the synchronizer at most. Contrast this result with the need to multiply the number of stages by 4, discussed above.

Designing for worst case, as suggested in this section, may result in extremely high latency, which may be prohibitive in some applications. As is evident from the previous examples, synchronization parameters are functions of supply voltage and temperature. These parameters tend to change dynamically during functional operation. Since a large number of flip-flops is needed only in corner cases, it is possible to dynamically adapt the number of synchronization stages based on τ measurements (as presented, for instance, in [4]). With such an adaptation, a tradeoff between latency and reliability can be achieved for typical scenarios without compromising reliability in corner cases.

VI. Conclusions

We presented a model that is able to predict $MTBF$ for different levels of supply voltage and temperature. The model is based on a semi-empirical model developed for the resolution time constant τ and on an empirical model for the metastability window T_W. The τ model was shown to be highly accurate with respect to measurements and simulations, with errors below 2%. The model is based on five semi-empirical parameters ($A, \alpha, \alpha_{VThE}, \alpha_{\mu}, V_{ThE}$) which are obtained from curve fitting to simulated or measured data. The T_W model is based on six empirical parameters $(a_{1,1}, a_{2,2}, \tilde{a}_{1,2}, b_1, b_2, c)$, which are obtained by a non-linear least-square regression to simulated or measured values.

Models for τ, T_W and $MTBF$ were shown to provide accurate prediction of values relieving the need for simulations or measurements for different (T, V_{DD}) corners.

The concepts of TCM and VCM were introduced, which are useful to understand the sensitivity of $MTBF$ with respect to τ and T_W. Both VCM and TCM were studied. $MTBF$ sensitivity was shown to present worst case scenarios under low temperature and low supply voltage conditions, where the sensitivities to variations peaked.

Bounds for T_W were studied and their influence on $MTBF$ was evaluated. Both T_{Wmax} and T_{WTc} bounds were shown to provide less tight lower bounds on $MTBF$. Moreover, we showed that using the bounds to calculate the number of stages of a synchronizer may result in unnecessary large margins in the number of flip-flops to use compared to model calculations. The model presented was shown to predict the number of flip-flops in good correlation with simulations.

Based on the derived model, we proposed synchronizer

design guidelines to account for temperature and supply voltage variations.

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