An on-chip metastability measurement circuit to characterize synchronization behavior in 65nm

Salomon Beer[1,2], Ran Ginosar[1], Michael Priel[2], Rostislav (Reuven) Dobkin [1] and Avinoam Kolodny[1]
[1]EE Dept, Technion—Israel Institute of Technology, Haifa, Israel, [2]Freescale Semiconductor
{shloimi,mpriel}@freescale.com, {sbeer@tx, rostikd@tx,ran@ee, kolodny@ee}.technion.ac.il
Phone: ++(972)+9+9522529, Fax:++ (972) 99522888

Abstract

Recent synchronizer metastability measurements indicate degradation of MTBF with technology scaling, calling for measurement and calibration circuits in 65nm circuits and beyond. An on-chip metastability measurement circuit was fabricated in a 65nm 1.1V bulk CMOS. A fully digital on-chip measurement system is presented here that helps to characterize synchronizers in future technologies. Different types of synchronizers were measured and compared. The standard library FF is demonstrated to have lower tau value than various feedback flip-flops.

I INTRODUCTION

Large multiple-clock domains Systems on Chip (SoC) typically require synchronization when transferring signals and data among the various clock domains and when receiving asynchronous inputs. Such synchronizations are often susceptible to meta-stability effects [1], which may propagate into the receiving circuit and may cause malfunctioning. To mitigate the effects associated with metastability, latches and flips flops are often used to synchronize the data [2], such as an N+1 pipelined flip flops (Fig. 1), which reserve a pre-determined time S for metastability resolution, $S \approx N \times T_C$ (T_C is the clock cycle time of the receiving clock domain).

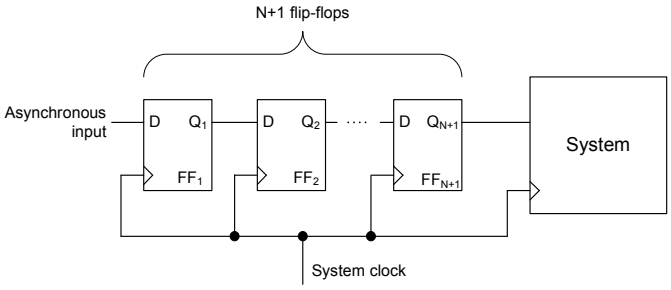


Figure 1. A typical synchronizer using N+1 cascaded flip flops

There is, however, a finite probability that the circuit will not resolve its metastable state correctly within the allowed time. To enable assessing the risk, and to enable the design of reliable synchronizers and systems, models describing the failure mechanisms for latches and flip flops have been developed [1][2][3] Most models express the risk of not resolving metastability in terms of the mean time between failures (MTBF) of the circuit (1).

$$MTBF = \frac{e^{S/\tau}}{T_W \times F_C \times F_D} \qquad (1)$$

Where F_C and F_D are the receiver and sender frequencies, respectively, τ is the resolution time constant, and T_W is a parameter often related to the setup-and-hold time window at the synchronizer input.

Desirable values of MTBF depend on the application and range from several years upwards. The parameter τ is predominant in synchronizer characterization since its effect on MTBF is exponential. Hence lower values of τ correspond to a "good" synchronizer while higher values to a "bad" one. Typical values of τ are the same order of magnitude as the gate delay of the technology (often expressed as FO4, the fanout-of-four delay of a standard gate). Evidently, as technology scales, FC and FD increase and to maintain high MTBF (without increasing N) τ must decrease as well.

In the past, τ was believed to improve with technology scaling [4]. However, recent measurements [5][6] indicate that scaling trends of synchronizers should be re-considered: The need to obtain full characterization will be imperative in technologies beyond 45nm. This paper describes a fully digital on-chip characterization circuit to measure synchronization performance. Our work also compares different synchronization circuits and demonstrates that the standard library flip flop achieves better performance relative to other solutions. To demonstrate the system, a 102x78 μm^2 on-chip digital measurement circuit was fabricated in a low power 1.1V 65nm bulk CMOS process (Fig. 9).

II PROPOSED CHARACTERIZATION METHOD

The measurement consists of sampling the output of the FF-under-test twice: first (X in Fig 2a) by the clock delayed by a factor DL (by means of a delay line) and second (Y) by the negative edge of the clock. The two samples are compared by a XOR gate. A metastability event that resolves during the time window between the delayed and negative edges of the clock (namely an event that did not resolve within the allotted time S) increments the counter (the number of events expected to resolve after the negative edge of the clock is negligible, since a low frequency clock is used). The measurement continues for time period T and thus MTBF is T divided by the counter value.

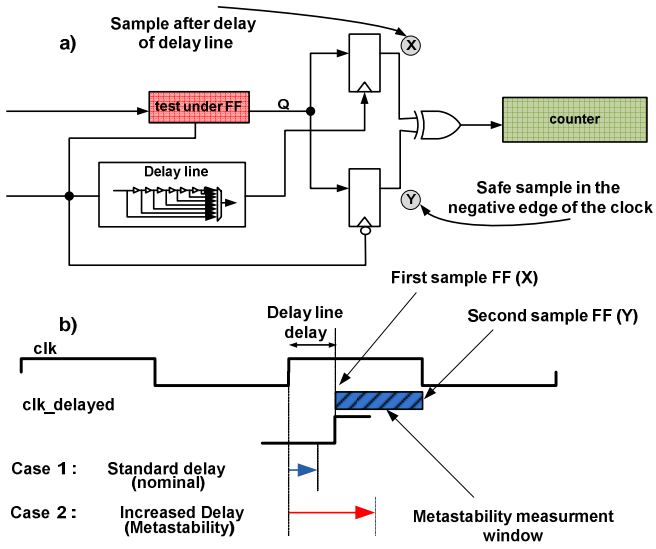


Figure 2 (a) Metastability measurement method (b) Waveforms explaining the operation of measuring method.

The entire measurement is repeated for different DL delays, obtaining a set of (DL,MTBF) readings. This set is used to compute τ, T_W . The method assures higher accuracy and 20% lower measurement noise compared to methods requiring variable high frequency clocks [5].

Figure 3 shows the complete on-chip measurement system which comprises a shift register that holds the configuration data, an input and clock generation unit (ICG), a design under test unit (DUT) that includes four different types of flip flops used as synchronizers, a measuring unit (ME) that includes the circuit of Fig 2(a), a 16-bit counter and an output serializer.

A controller writes into the shift register in order to configure the DUT and the DL value. The controller sets the measuring period T by enabling and disabling the counter. T can vary from seconds to hours. Following each measuring period, the controller initiates a serial readout of the counter value. This procedure is repeated for multiple values of DL. The entire test is performed under software control, and readings are further processed by the software.

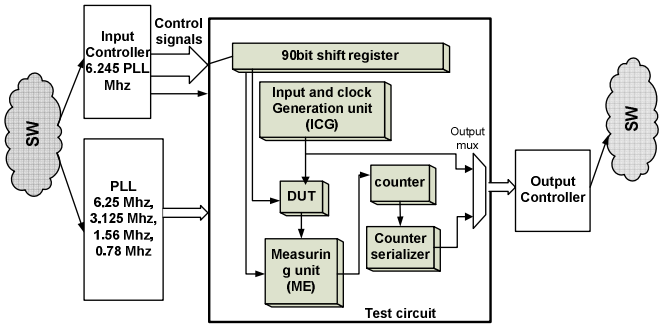


Figure 3. Block diagram of the metastability measurement circuit and system.

The test system employs a single output pin and six input pins; in practice, such a system could be designed as fully-contained built-in test without any dedicated external pins. The measurement unit area is 290 μm^2 and its power consumption is negligible.

III SYNCHRONIZER COMPARISON

In order to validate the operation of the measurement circuit different types of flip flops (FFs) were tested and characterized (Fig 4): The regular library FF, the TG feedback FF [7], the XOR feedback FF [8] and the delayed XOR feedback FF [8]. In an attempt to improve (to lower) τ, several circuit designs were proposed. τ is modeled as $\tau = C/g_m$ where C is the output capacitance and g_m is the trans-impedance of the master latch in the synchronizing FF.

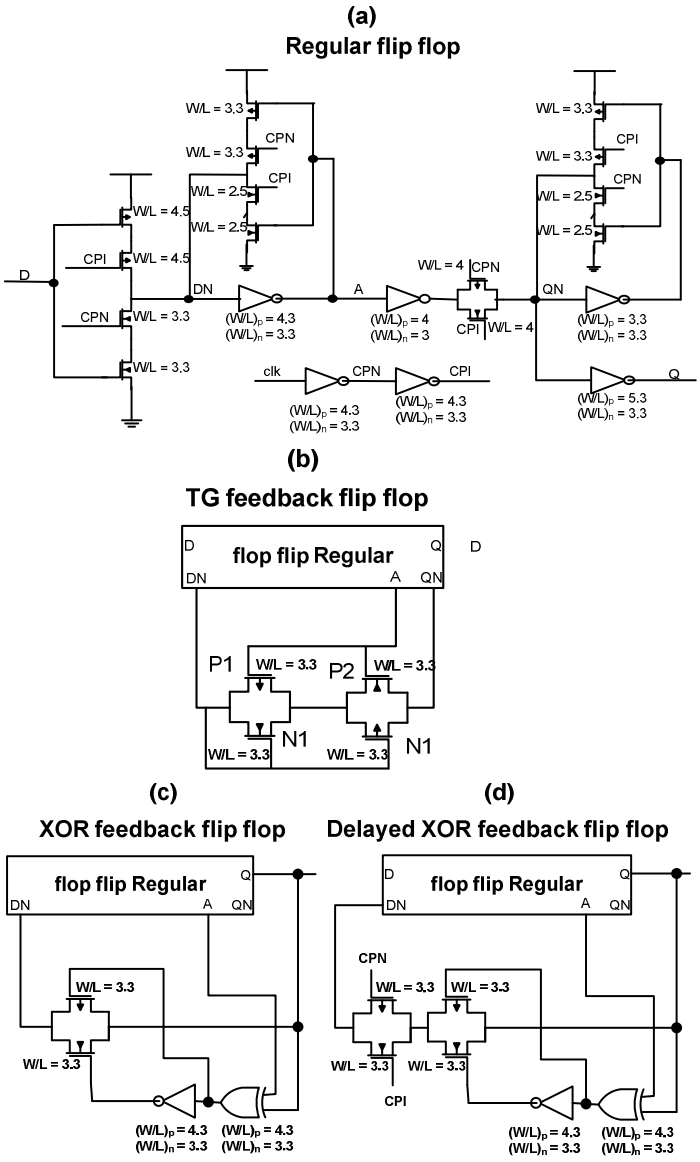


Figure 4. Schematics of the tested synchronization flip-flop circuits (a) regular library FF (b) TG feedback FF (c) XOR feedback FF (d) Delayed XOR feedback FF.

The main purpose of each circuit, is to increase significantly the value of g_m in the master latch during metastability and hence to reduce τ, for that purpose, they employ a feedback arrangement comprising a transmission gate circuit that conducts only when the output node of the master latch in the FF is in a mid-voltage state.

The regular library FF employs enabled (three-state) inverters (Fig 4a). The operation of the flip-flop is as follows: A signal at the D input is inverted through the enable inverter to node DN when the "master" clock CPI is low (and CPN high). The inverter of the master latch propagates the signal to node A. The feedback enable inverter of the master latch provides positive feedback that holds the voltage at DN at its previous state when signal CPI is high (and CPN low). The signal on node A is passed through an inverter and a transmission gate when the "slave" clock signal CPI is high (and CPN low). The inverters of the slave latch provide the output signal Q. The enabled inverter in the slave provides for latching signal Q when CPN is high (and CPI low). The net result is that either a low or high logic level (e.g., V_{SS} or V_{DD}) as the D input is latched at the Q output when the clock CPN goes low. Thereafter, the Q output can not change state until the next high to low transition of the CPN clock. (low to high transition of the clk signal)

A problem with latch circuitry occurs when the voltage at the D input changes at the same time that the clock signal CPI/CPN makes its low-to-high/high-to-low transition. If the D input is making a low-to-high transition at that moment, then it is indeterminate whether a low or high voltage will appear at the DN point and hence in the Q output. In fact, DN may remain at an intermediate state midway between the logic levels for an indefinite period of time, i.e. enters metastable state. The time necessary to resolve the output, that is, to go to either a high or low stable state, is a measure of the effectiveness of the overall design of the latch circuitry. (τ)

In order to overcome the metastability problem, improved flip-flops were proposed (Fig. 4b,4c,4d) In normal condition, i.e. when the timing constraints are not violated, the circuit behaves as a regular flip-flop. In the transmission gate (TG) feedback FF, comprising P1, P2, N1, N2 transistors, one of two pairs of transistors (P1, N1 or P2, N2) will be cut off. The reason is that PMOS and NMOS transistors are connected in serial, and their gates are tied together. Thus if the gate voltage is either "1" or "0" one of the transistors will conduct current, and other will be cut off. The PMOS and the NMOS transistors that are connected in parallel have opposite potential at their gates. Thus both transistors in such parallel pair will be either conducting or cut off. Therefore, the voltage on the output node Q is not coupled to the input. However, when input node D is in an intermediate state between V_{DD} and V_{SS} when clock CPN goes low. In that case, an intermediate voltage between V_{DD} and V_{SS} will be produced on gates of transistors P1, P2, N1, N2. Either pair P1, P2 or N1, N2 will conduct (depends on a voltage of output node Q) and the feedback path from Q to D will be created, thus helping the master latch to resolve from metastability. For example if the Q voltage is V_{DD}, and the master latch is metastable, then the feedback path will be formed by P1 and P2. On the other hand, if the output voltage Q is low, the feedback path will be formed by N1, N2. This feedback will force the input voltage of the master latch towards the output voltage Q.

The XOR feedback FF and the delayed XOR feedback FF, are variants of the TG feedback FF using a XOR gate in order to improve trans-impedance in the master latch when the FF is in metastability.

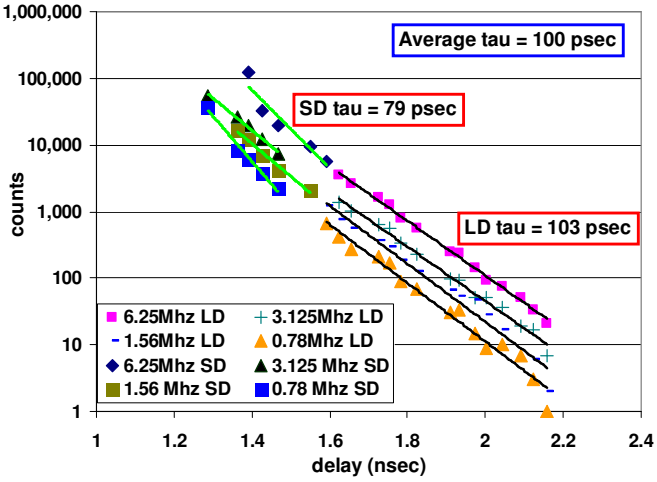
Aspect ratio of all transistors is indicated in Fig. 4, all transistors have minimum channel length. FF bulks are connected to ground and v_{DD} for NMOS and PMOS respectively.

IV RESULTS

Measurements were performed at v_{DD}=1.1V and room temperature, four data frequencies F_D=6.245Mhz, 3.125Mhz , 1.56Mhz and 0.78Mhz, and clock frequency F_C of 6.25Mhz. Each measurement period T lasted two minutes for each DL value. Measured values of the regular library FF, in the DL range of 1.3—2.15 nsec are presented in Fig. 5, showing exponential relation of resolution time to the number of events, as well as the computed values of τ . Two regions were identified, corresponding to short delay (SD) and long delay (LD), for better fit of the exponential parameters, as proposed in [3]. All measurements yielded consistent results for τ in the range 96–103psec as shown in Fig. 6. Characterization yielded a τ value of 101psec with 4% error.

The comparison results for the different types of FFs are charted in Fig 7, indicating that the regular library flip flop outperforms the other ones, namely it demonstrates lower τ . However the XOR feedback FF performs better than the TG feedback FF and the delayed feedback FF. The measurement results show that the proposed test structure measures a τ of 101psec for a regular library FF, 210psec for the TG FF, 148psec for the XOR FF and 168psec for the delayed XOR FF. These results can be accounted for by the fact that increasing input capacitance of the master latch has negative effect on τ , which counteracts any contribution of the feedback loops.

This effect is also corroborated by simulation (Fig 8) that provide further demonstration of the validity of the measurements.



. Figure 5 **Metastability event counts as a function of resolution delay and the resulting synchronization time constant (τ) overall and region estimates for the regular library flip-flop circuit.**

Figure 8 shows SPICE simulations comparing the regular library FF and the TG feedback FF, the method used for simulation is the same as [3][6]. The results show that regular FF resolves metastability faster than the TG feedback FF and thus corroborates our measurements.

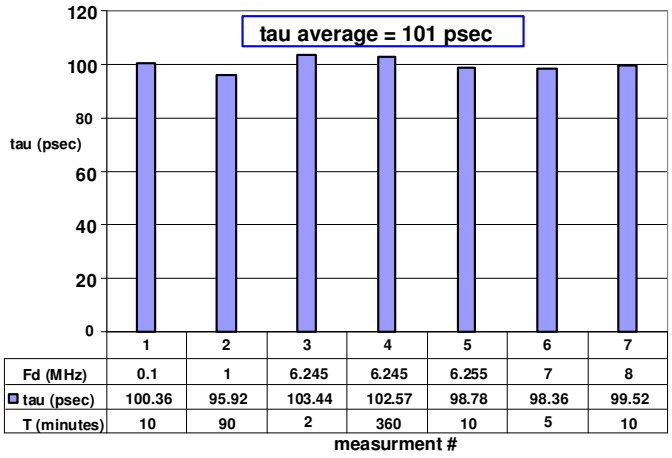


Figure 6. Measured τ for different data frequencies, and measurement periods of the regular library flip flop.

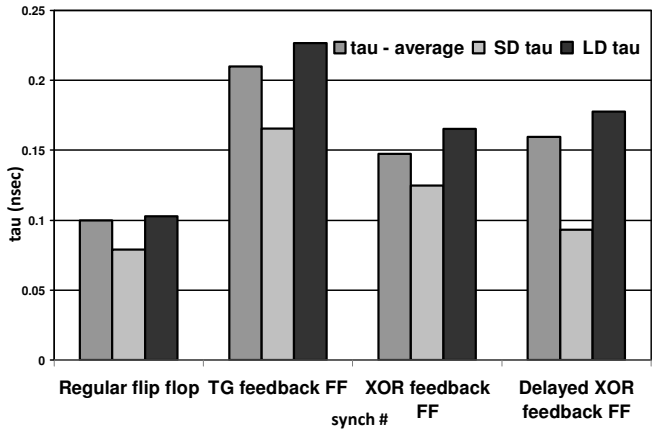


Figure 7 Metastability resolution performance comparison of the tested flip-flop circuits.

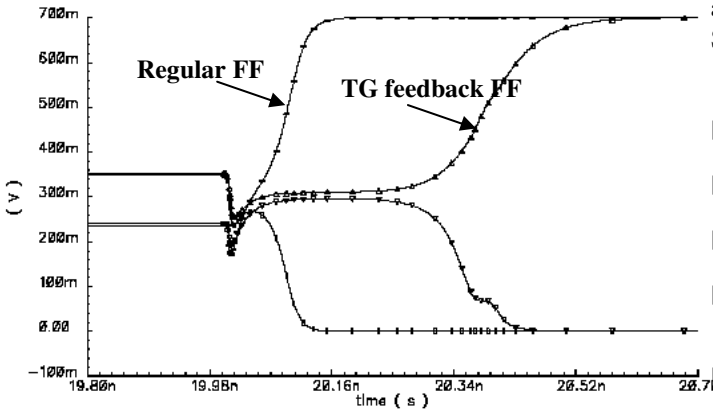


Figure 8 Simulation result of the regular FF and feedback FF

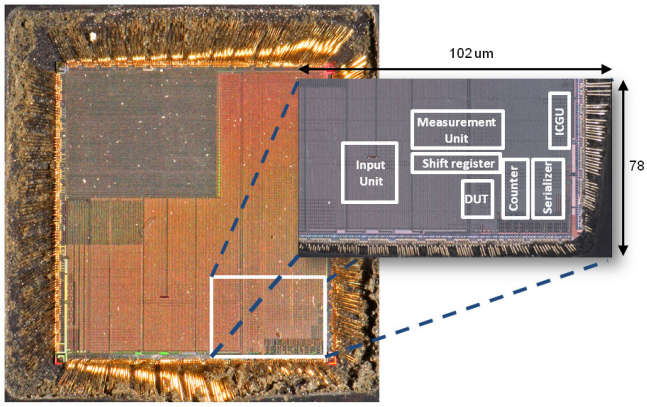


Figure 9. Micrograph of the metastability measurement circuit fabricated in 65nm CMOS.

V SUMMARY

The measurement results show that the proposed test structure extracts synchronization parameters in a 65nm process with high efficiency and very low test time and cost, thus validating the feasibility and usefulness of the proposed built-in-test scheme. It is also useful for fast and accurate process characterization during technology development.

Since the measurement circuit requires only two constant frequency sources and produces a digital output, it can be applied to a self-calibrating synchronizer design, which can be adjusted automatically and dynamically to varying circumstances such as process variations and environmental conditions (voltage and temperature), as well as to DVFS systems where voltage and clock frequencies may vary from time to time. Such self-calibration circuit may change the number of series FFs included in the synchronizer in order to assure the desired level of reliability under changing conditions.

VI ACKNOWLEDGMENT

The authors wish to thank Freescale Semiconductor for allowing the inclusion of the test circuit in one of their 65nm SoC.

VII REFERENCES

[1] L. Kleeman and A. Cantoni, "Metastable behavior in Digital Systems", IEEE Design & Test of Computers, 4, 6, 4-19, 1987.

[2] T. J. Gabara, "Metastability of CMOS Master/Slave Flip-Flops", IEEE CICC 1991.

[3] C.Dike and E. Burton, "Miller and noise effects in synchronizing flip-flop" IEEE JSSC, Vol. 34 No. 6, pp. 849-855, June 1999.

[4] M.S. Baghini, M.P Desai, "Impact of technology scaling on metastability performance of CMOS synchronizing latches", Proceedings of ASP-DAC/VLSI Design 2002. pp.317-22,2002.

[5] P. Alfke, http://forums.xilinx.com/t5/PLD-Blog/Metastable-Delay-in-Virtex-FPGAs

[6] S.M. Beer, R. Ginosar, M. Priel, R. Dobkin, A. Kolodny, "The Devolution of synchronizers", Proceedings of the ASYNC 2010., in press.

[7] Ronald L. Freyman, "Latch circuit with reduced metastability", US Patent 5081377, 1992.

[8] S.M. Beer, M.Priel, D. Kuzmin, "A device having synchronizing capabilities and a method for synchronizing" US12/113216 2008