An Extended Metastability Simulation Method; Extended Nose Short Simulation (ENSS)

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Abstract— **Synchronizers play a key role in multi-clock domain systems on chip. One of the essential points in designing reliable synchronizers is to estimate and evaluate synchronizer parameters τ and T_W . Typically, evaluation of these parameters has been done by empirical rules of thumb or simple circuit simulations to ensure that the synchronizer MTBF is sufficiently long. This paper shows that those rules of thumb and some common simulation method are unable to predict correct synchronizer parameters in deep sub-micron technologies. We propose a new simulation method to estimate synchronizer characteristics more reliably and compare the results obtained with other state of the art simulation methods. Simulation results for each of the analyzed methods are compared with measurements of a 65nm LP CMOS test-chip.**

1 INTRODUCTION

Multiple-clock domain System on Chip (SoC) designs requires synchronization when transferring signals and data among clock domains and when receiving asynchronous inputs. Such synchronizations are susceptible to metastability effects [1][2] which can cause malfunction in a receiving circuit. In critical designs, this risk must be mitigated. To assess the risk and to design reliable synchronizers, models describing the failure mechanisms for latches and flip-flops have been developed [3][4] . Most models express the risk of not resolving metastability in terms of the mean-time-between-failures (MTBF) of the circuit,

$$MTBF = \frac{e^{S/\tau}}{T_W \times F_C \times F_D} \quad (1)$$

where S is the time allotted for resolution, F_C and F_D are the receiver and sender frequency, respectively, τ is the resolution time constant, and T_W is a parameter related to the effective setup-and-hold time window during which the synchronizer is vulnerable to metastability.

Over the years, techniques have been developed for obtaining an arbitrarily long MTBF. These techniques have been translated into convenient rules of thumb for designers. As digital circuits have become more complex, denser and faster with reduced power consumption, the old rules of thumb are beginning to fail [5][6], especially when adding process variations and operating-condition sensitivities in today's manufacturing technologies [7]. Until now, a rule of thumb has been that the time constant τ is proportional to the fan-out of four FO4 propagation delay. This rule of thumb predicts that τ decreased as feature size and FO4 gate delay decrease. However, a change in this pattern is emerging at process nodes 90nm and below [5][6][8]. This change is particularly significant when the metastable voltage (typically about $½V_{DD}$) is in the vicinity of the transistor threshold voltage, an increasingly common occurrence for low-power circuits. Under these circumstances, the current flowing in a metastable complementary pair of transistors can be exceedingly small [6], resulting in a large value of τ. Operating conditions, particularly at low temperatures, and process variations further aggravate the situation and can cause many orders of magnitude variation in the MTBF of a synchronizer. No longer can the designer depend upon the rule of thumb that τ is proportional to the FO4 delay. As a result, traditional guidelines for synchronizer design are no longer useful. Desirable values of MTBF depend on the application and range from several years upwards.

Over the years, several simulation methods have been proposed. In some works [4][5][12], the simulation shorts latch nodes to force metastability in order to estimate τ. The purpose of this work is to show that this method is accurate only for the case of symmetric cross-coupled inverters in latches and fails to produce correct results in any other case. We then extend the method for the case of asymmetric cross-coupled inverters and compare the results of our extended method to results received with two other state of the art simulation methods. We also provide a comparison of those simulations with real measurements of 65nm LP CMOS flip-flops.

2 SHORTING NODE SIMULATION METHOD

Shorting nodes simulation is used in [4][5][12]. This method shorts the two nodes of a latch (Figure 1) to equate their voltage and then breaks the short and allows resolution. When the switch is opened, the voltage nodes diverge exponentialy. When two inverters are cross connected, it is possible to describe their behavior by

$$\begin{aligned} \tau_a \dot{v}_a(t) &= -(v_b(t) - v_{ma}) \\ \tau_b \dot{v}_b(t) &= -(v_a(t) - v_{mb}) \end{aligned} \quad (2)$$

where the time constant $\tau_i = C_i/g_{mi}$, v_{mi} is the metastability voltage at the input of the i^{th} inverter, C_i is the total capacitance associated with the i^{th} output node, g_{mi} is the transconducntance of the i^{th}inverter and $i = a, b$.

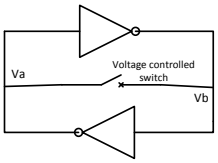

Figure 1. Shorting latch nodes

In particular, if the cross-coupled inverters are symmetric, $\tau_a = \tau_b = \tau$, $v_{ma} = v_{mb}$ and in terms of the difference voltage $v_D(t) = v_a(t) - v_b(t)$ we get $\tau \dot{v}_D(t) = v_D(t)$ whose solution is

$$v_D(t) = v_D(0)e^{t/\tau} \tag{3}$$

From the transient simulation of the resolving nodes, the exponential rate of divergence of the two nodes, τ, is computed. The result of such a simulation using circuit of Figure 1 with equal inverters is shown in Figure 3, at time 1nsec the voltage controlled switch is opened and nodes V_a and V_b diverege to opposite directions. The natural logarithm of the voltage difference $v_D(t)$ is ploted in blue, clearly showing an exponential resolution with time as predicted by (3). The inverse of the derivative of the blue line is shown in green yielding τ. The flatness of the green line, corresponds with our model of the diverenge being exponential.

Without the assumption of symmetry, the solution of (2) becomes

$$\begin{aligned} v_a(t) - v_{mb} &= v_{1+}e^{t/\tau} + v_{1-}e^{-t/\tau} \\ v_b(t) - v_{ma} &= v_{2+}e^{t/\tau} + v_{2-}e^{-t/\tau} \end{aligned} \tag{4}$$

The constants $v_{1+}, v_{1-}, v_{2+}, v_{2-}$, are determined by initial conditions and depend on when the origin of the time scale is set and $\tau = \sqrt{\tau_a \tau_b}$. In this case, shorting the inverted nodes does not produce a metastable state in the latch, and hence this simple procedure cannot be used to simulate τ. Figure 4 shows simulation using a latch with non-symmetric inverters. The color code for the plots follows that of Figure 3. The green plot is not flat showing not simple exponential behavior, and hence τ cannot be computed from the slope of natural logarithm of the voltage difference.

When the cross-coupled inverters are symmetric (Figure 6(a)), the metastable point lies on the line $V_a = V_b$, so when the nodes are shorted, the system is placed into metastability (blue circle). On the other hand, when the cross-coupled inverters are asymmetric (Figure 6(b), skewed low, or Figure 6(c), skewed high), the metastable point is not obtained by shorting the two nodes. When the switch is opened, the latch follows the green path through the state space, from the blue circle on $V_a = V_b$ towards either the (1,0) state (Figure 6(b)) or the (0,1) state (Figure 6(c)).

3 Extension of Shorting Node Simulation Method

In an asymmetric latch, the metastable voltages of the two nodes differ by some V_{diff} (Figure 2), which needs to be found. If a voltage source $V_S = V_{diff}$ is placed between the two nodes (Figure 2), the latch is forced into metastability. Figure 5 shows simulation plots for an asymmetic latch using circuit of Figure 2. V_{diff} is found and V_s is set to its value, then the switch is released showing the exponential behavior predicted by (4). Note that the current through the switch is zero, and thus the switch can be openeded without changing any condition.

An iterative simulation process is employed to find the desired value of V_{diff}. An adjustable voltage source V_s is used, and its value is changed until V_s=V_{diff}, namely until the metastable point lies on the line $V_s = V_{diff} = V_a - V_b$ (Figure 2).

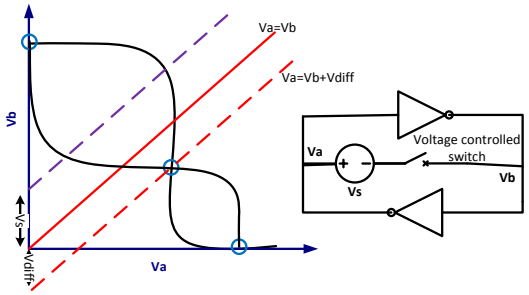

Figure 2. **Proposed technique for reaching metastability in asymmetric latches**

Three alternative iterative procedures are proposed, as follows:

a) VTC diagrams (voltage transfer curve)
b) Bisection
c) Current compensation

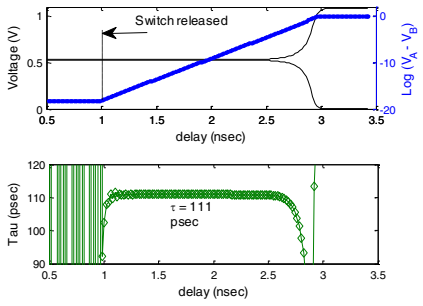

Figure 3. Short simulation of symmetric latch.

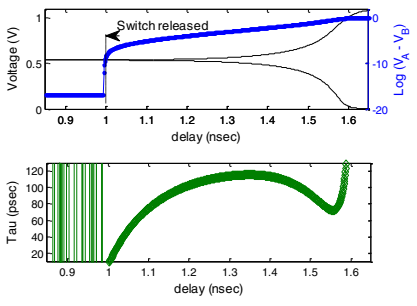

Figure 4. Short simulation of asymmetric latch.

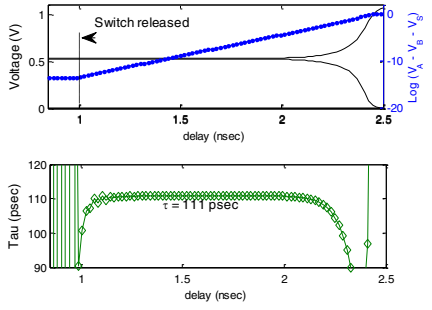

Figure 5. Extended short simulation of asymmetric latch

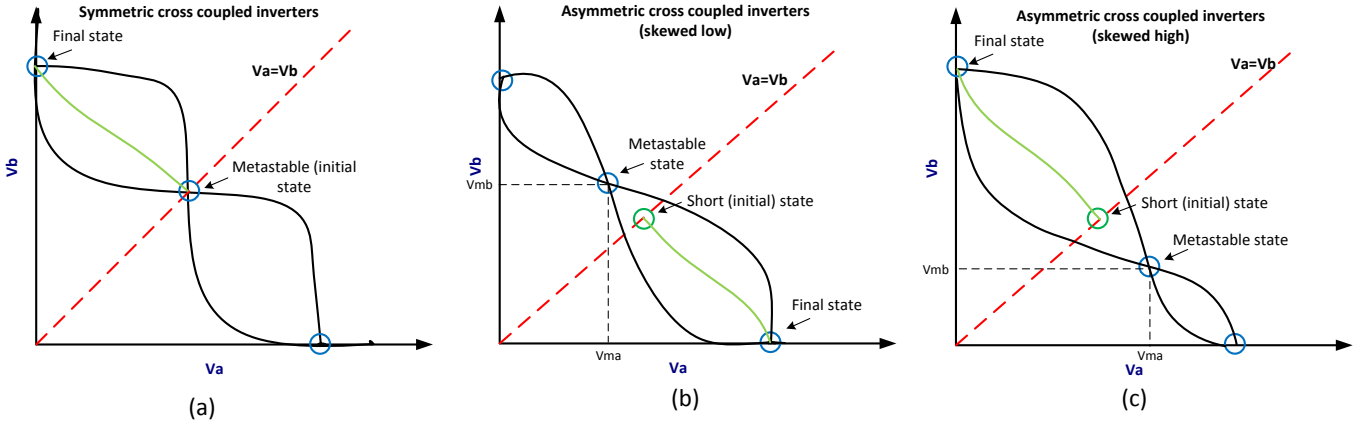

Figure 6. **(a) Symmetric cross-coupled inverters. (b)skewd low asymmetric cross-coupled inverters. (c) skewed high asymmetric cross-coupled inverters.**

In the VTC diagram approach, the VTC of each inverter in the cross-coupled latch is generated, using DC sweep simulations, and their intersection, which is the metastable point, is found, similarly to Figure 6. In the Bisection method, we first start by choosing two values for V_s, $\{V_{s1,0}, V_{s2,0}\}$ that, when using transient simulations of the circuit in Figure 2, lead to two opposite transitions of the node V_a (or V_b).

The interval $[V_{s1,0}, V_{s2,0}]$ contains the metastable point of the circuit. Then we find a narrower, enclosed interval $[V_{s1,1}, V_{s2,1}]$ that also produces two opposite transitions on its extremes. By construction, $V_{diff} \in [V_{s1,1}, V_{s2,1}]$. Following this procedure iteratively it is possible to find an arbitrarily small interval $[V_{s1,n}, V_{s2,n}]$, that contains the meteastable point after n interations of the algorithm. In this way we are able to find the metastable point with as high accuracy as desired.

The current compensation method adjusts the voltage V_s with the switch closed. If $V_s > V_{diff}$, current flows in one direction, and if $V_s < V_{diff}$, current flows in the opposite direction. Iteratively adjust V_S until the current is zero. At that stage, $V_s = V_{diff}$ and the latch is metastable.

Generating VTC diagrams incurs less computation than the bisection method. Only DC sweep simulations are needed, and V_{diff} can be calculated with high accuracy. While the bisection method requires several transient SPICE simulations with fine resolution and long run time, the current compensation method requires a similar number of simpler DC simulations. The major drawback of the VTC method is that it requires breaking the circuit into subparts, and simulating each part separately. The bisection and current compensation methods require access to flip-flop internal nodes (so called "antenna nets").

The drawback of shorting nodes simulation method is its inability to simulate the paremeter T_W. In most cases, however, knowing the value of τ is sufficient to reliably estimate the failure probability.

4 Simulations and Measurements

In this section we present measurements of a library master-slave flip-flop (Figure 7), used as a synchronizer in a 65nm LP CMOS process, and compare the results to simulations using our extended short simulation method. The library flip flop is asymmetric due to different loading in the master latch nodes. We also compare simulations generated by our extended shorting node simulation method to the results generated by two other state of the art simulation methods. The sweep simulation method described in [15][16] and the parametric simulation method presented in [17].

All simulations were performed using SPICE BSIM4 model level 54. The measurement method used was the one shown in [18] A comparison of τ in measurements and in simulations is presented graphically in Figure 8 for different supply voltages between 0.95V to 1.3V.

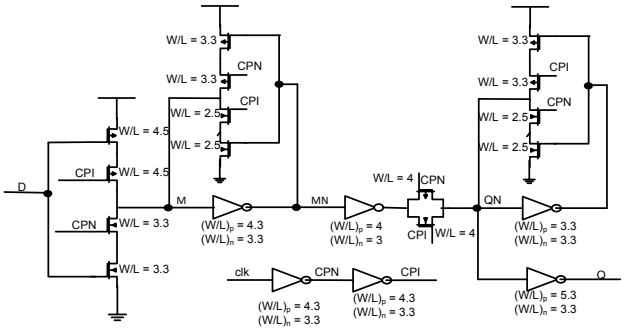

Figure 7. **Library flip-flop used for simulation and measurements.**

A comparison of the run times for ENSS simulation and the sweep simulation is shown in Fig. 9. For a fair comparison all simulations were performed using a common maximum resolution time (T_S). The V_{diff} resolution of ENSS was previously calibrated for T_S. This is why for higher supply voltages, for which τ is lower, more iterations

are required to achieve the target resolution time and hence the run time is higher. The results show that our method provides accurate results much faster than the sweep and parametric method

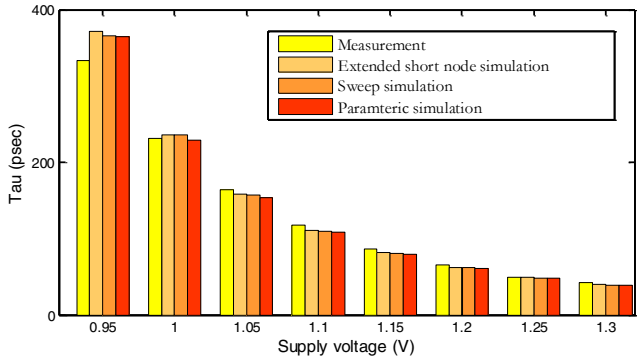

Figure 8. τ **vs supply voltage, for measurements and simulations of a library 65nm CMOS FF.**

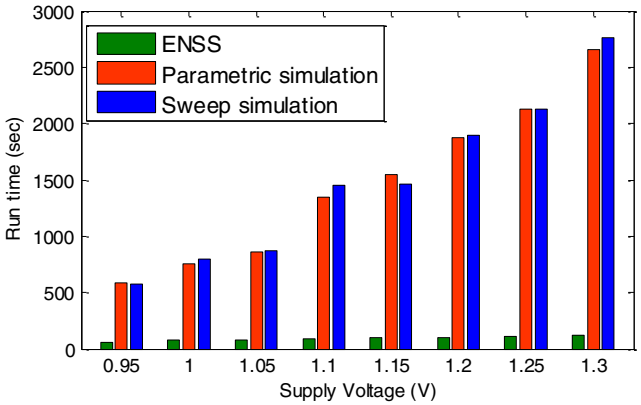

Fig. 9. Run times for ESNS simulation method and sweep simulation method

The displacement of the metastable point from the symmetrical case, V_{diff}, is shown against supply voltage in Figure 10. Note that V_{diff} is never zero along this range of supply voltages, and strongly depends on the supply voltage.

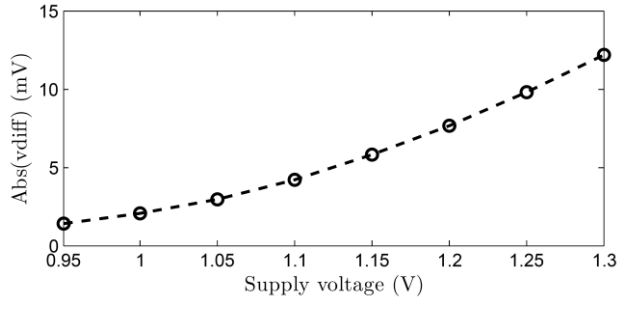

Figure 10. Displacement of metastable point (V_{diff}) against supply voltage using shorting nodes simulation

5 Conclusions

We demonstrated that the shorting nodes method as previously used in the literature is inappropriate for simulating asymmetrical latches. We extended the short node simulation method to yield correct results in the case of asymmetric latches and showed that the methods yields correct simulation results. We showed three different methods of calculating the metastable voltage, using VTC, bisection and current compensation. We also compared the results of our extended simulation method with sweep and parametric simulation methods and showed that the results match. We proved our simulation method against measurements taken from a circuit fabricated in a CMOS LP 65nm process. Simulation results predict τ with an error of less than 12% (measurement equipment error) compared to measurements so demonstrating it is suitable to characterize synchronizers in a reliable and easier way.

6 References

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