An Extended Metastability Simulation Method for Synchronizer Characterization

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Abstract. Synchronizers play a key role in multi-clock domain systems on chip. Designing reliable synchronizers requires estimating and evaluating synchronizer parameters $\boldsymbol{\tau}$ (resolution time constant) and $\boldsymbol{T_W}$ (metastability window). Typically, evaluation of these parameters has been done by empirical rules of thumb or simple circuit simulations to ensure that the synchronizer MTBF is sufficiently long. This paper shows that those rules of thumb and some common simulation method are unable to predict correct synchronizer parameters in deep sub-micron technologies. We propose an extended simulation method to estimate synchronizer characteristics more reliably and compare the results obtained with other state-of-the-art simulation methods and with measurements of a 65nm LP CMOS test-chip.

Keywords: Synchronization, metastability, synchronizers, simulation, MTBF.

1 Introduction

Multiple-clock domain System on Chip (SoC) designs require synchronization when transferring signals and data among clock domains and when receiving asynchronous inputs. Such synchronizations are susceptible to metastability effects which can cause malfunction in a receiving circuit. In critical designs, this risk must be mitigated. To assess the risk and to design reliable synchronizers, models describing the failure mechanisms for latches and flip-flops have been developed [1][2]. Most models express the risk of not resolving metastability in terms of the mean-time-between-failures (MTBF) of the circuit, Eq. (1), where S is the time allotted for resolution, F_C and F_D are the receiver and sender clock frequencies, respectively, τ is the resolution time constant, and T_W is a parameter related to the effective setup-and-hold time window during which the synchronizer is vulnerable to metastability.

$$\mathrm{MTBF} = \frac{e^{S/\tau}}{T_W \times F_C \times F_D} \tag{1}$$

Over the years, techniques have been developed for obtaining an arbitrarily long MTBF. These techniques have been translated into convenient rules of thumb for designers. As digital circuits have become more complex, denser and faster with

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reduced power consumption, the old rules of thumb are beginning to fail [3][4], especially when adding process variations and operating-condition sensitivities in today's manufacturing technologies [5]. One rule of thumb has stated that the time constant τ is proportional to the fan-out of four (FO4) propagation delay. This rule of thumb thus predicts that τ decreases with feature size and FO4 gate delay. However, a change in this pattern is emerging at process nodes 90nm and below [3][4][6]. This change is particularly significant when the metastable voltage (typically about ½V_{DD}) is in the vicinity of the transistor threshold voltage, an increasingly common occurrence for low-power circuits employing lower supply voltage and high threshold transistors. Under these circumstances, the current flowing in a metastable complementary pair of transistors can be exceedingly small [4], resulting in a large value of τ. Operating conditions, particularly at low temperatures, and process variations further aggravate the situation and can cause many orders of magnitude variation in the MTBF of a synchronizer. No longer can the designer depend upon the rule of thumb that τ is proportional to the FO4 delay. As a result, traditional guidelines for synchronizer design are no longer useful and simulations should be used to correctly estimate synchronizer error probabilities.

Over the years, several simulation methods have been proposed to calculate synchronizer failure probabilities. In some works [2][3][7], the simulation shorts latch nodes to force metastability to estimate τ. In this work we show that this simple node-shorting method is inadequate for simulating general latches and is only valid for fully symmetric cross-coupled inverters. In non-symmetric latches the method generates incorrect results. Typically, a chain of latches or flip-flops is used for synchronization. Those latches are usually non-symmetric or the capacitive loading by other circuits leads to non-symmetric circuits, yielding inaccurate results. We propose an extension of the simulation method for the case of asymmetric cross-coupled inverters and compare the results of our extended method to results obtained by two other state-of-the-art simulation methods [8][10]. We show that our proposed novel simulation method correctly predicts synchronizer parameters in a simpler manner and at a lower computational cost than another recently published method [8]. To further validate our method we also compare the result of our simulations with real measurements of 65nm LP CMOS latches.

2 Node Shorting Simulation

Node shorting simulation (NSS), as described in [2][3][7], is widely used by designers. The two nodes of a latch are shorted to equate their voltage, simulating metastability. When the short is opened, the latch is allowed to resolve. One node will diverge to V_{DD} while the other to ground. A small battery (order on nV) across the nodes is placed to ensure the starting time and the direction of divergence. Fig. 1 shows two different latch configurations with the voltage controlled switch that is used to short the lacth nodes (dotted lines). The potential metastable nodes a, b are higlighted in red.

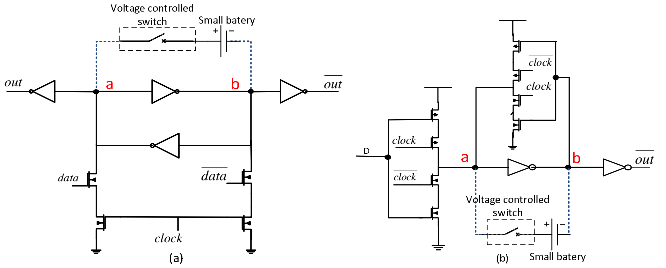

Fig. 1. Two common latch configurations, (a) Reduced clock swing latch [12] (b) regular low high latch configurations [13]

The small signal behavior of the latch can be modeled as two cross coupled inverters as shown in [7][10] and it is possible to describe their behavior by

$$\begin{aligned}\tau_a \dot{v}_a(t) &= -(v_b(t) - v_{ma})\\ \tau_b \dot{v}_b(t) &= -(v_a(t) - v_{mb})\end{aligned} \tag{2}$$

where the time constant $\tau_i = C_i/g_{mi}$, v_{mi} is the metastability voltage at the input of the i^{th} inverter(in the metastable node), C_i is the total capacitance associated with the i^{th} metastable node, g_{mi} is the trans-conductance of the i^{th}inverter and $i = a, b$. In particular, if the cross-coupled inverters are symmetric, $\tau_a = \tau_b = \tau$, $v_{ma} = v_{mb}$ and in terms of the difference voltage $v_D(t) = v_a(t) - v_b(t)$ we get $\tau \dot{v}_D(t) = v_D(t)$ the solution of which is

$$v_D(t) = v_D(0)e^{t/\tau} \tag{3}$$

From a transient simulation of the resolving nodes $(v_D(t))$, the exponential rate of divergence τ can be computed. The result of such a simulation using a symmetric latch circuit as the one shown in Fig. 1a (symmetric inverter and same size transistors with respect to nodes *a,b*) is shown in Fig. 2. At 1nsec the voltage controlled switch is opened and nodes V_a and V_b diverge to opposite directions (black solid lines). The logarithm of the voltage difference $v_D(t)$ is plotted in blue, clearly showing an exponential resolution in time as predicted by Eq. (3). The inverse of the derivative of the blue line is shown in green yielding τ. The flatness of the green line corresponds with Eq. (3).

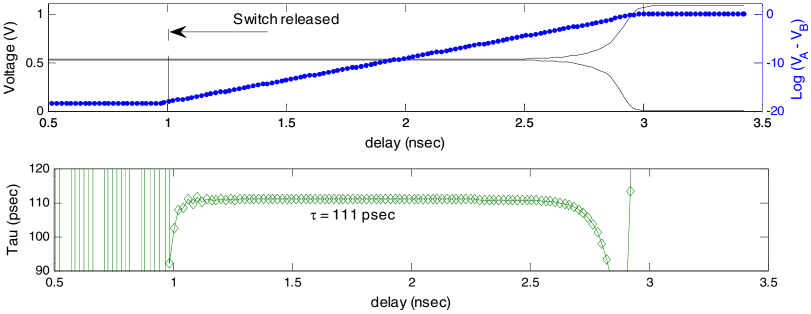

Fig. 2. Node shorting simulation for symmetric latch shown in Fig. 1a

Without the assumption of symmetry in the latch, the general solution of Eq. (2) is

$$v_a(t) - v_{mb} = v_{1+}e^{t/\tau} + v_{1-}e^{-t/\tau}$$
$$v_b(t) - v_{ma} = v_{2+}e^{t/\tau} + v_{2-}e^{-t/\tau} \quad (4)$$

The constants $v_{1+}, v_{1-}, v_{2+}, v_{2-}$, are determined by initial conditions and depend on the setting of origin of the time scale and $\tau = \sqrt{\tau_a \tau_b}$. In this case, shorting the nodes does not force a metastable state in the latch, and hence this simple procedure cannot be used to simulate τ. Fig. 3 shows a simulation using the latch configuration of Fig. 1a with non-symmetric inverters, using the same color code as in Fig. 2. The green plot is not flat, showing non simple exponential behavior and hence τ cannot be computed from the slope of the logarithm of the voltage difference as proposed by the simple short node simulation method.

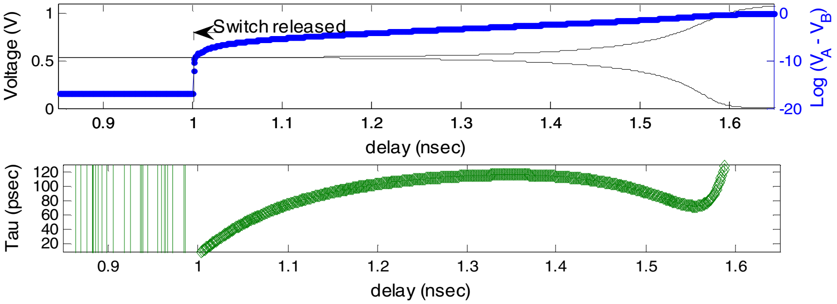

Fig. 3. Node shorting simulation of non-symmetric latch of Fig. 1a

When the cross-coupled inverters and capacitance loading are symmetric in the circuit of Fig. 1a, the metastable point lies on the line $V_a = V_b$ (Fig. 4a) and when the nodes are shorted the system is forced into metastability (blue circle). On the other hand, when the cross-coupled inverters are non-symmetric (Fig. 4b, skewed low, or Fig. 4c, skewed high), the metastable point is not reached by shorting the two nodes. Instead, shorting the two nodes yields an intermediate state (green circle), different than the metastable state (blue circle); when the switch is opened, the latch follows the green path in state space, from the blue circle on $V_a = V_b$ towards either the (1,0) state (Fig. 4b) or the (0,1) state (Fig. 4c).

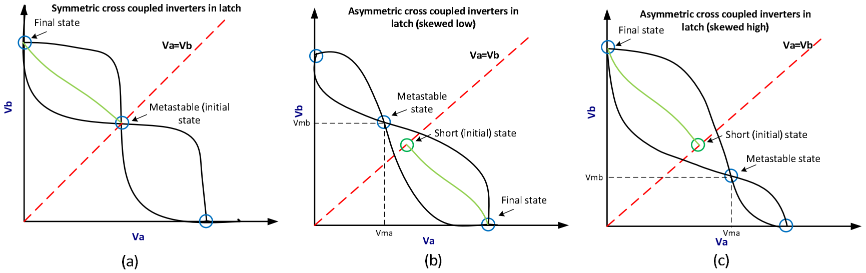
Symmetric cross coupled inverters in latch
Final state
Va=Vb
Metastable (initial state
Vb
Va
(a)
Asymmetric cross coupled inverters in latch (skewed low)
Va=Vb
Metastable state
Short (initial) state
Final state
Vb
Vmb
Vma
Va
(b)
Asymmetric cross coupled inverters in latch (skewed high)
Final state
Va=Vb
Short (initial) state
Metastable state
Vb
Vmb
Vma
Va
(c)

Fig. 4. Voltage transfer curves (VTC) (a) Symmetric latch (b)skewd low asymmetric latch (c) skewed high asymmetric latch

3 Extended Node Shorting Simulation

In an asymmetric latch, the metastable voltages of the two nodes differ by some V_{diff} (Fig. 5a), which needs to be found. Using the notation of (4), $V_{diff} = v_{ma} - v_{mb}$. If a voltage source $V_S = V_{diff}$ is placed between the metastable nodes, shown in Fig. 5b, when the switch is closed the latch is forced into metastability (blue circle). Then the switch can be released showing the exponential behavior predicted by Eq. (4). In the case when the value of V_S is exactly V_{diff} the current through the switch is zero, and thus the switch can be opened without changing any condition. This is caused because the intrinsic difference between the metastable voltages of the nodes (V_{diff}) is compensated for by the voltage source $V_S = V_{diff}$, resulting in no current through the switch.

Consequently our enhanced node shorting simulation (ENSS) method comprises two steps:

(i) Finding the metastability offset voltage (V_{diff}).
(ii) Node shorting transient simulation as described in Sec. 2 using $V_S = V_{diff}$.

An iterative process is used to find the value of V_{diff}. An adjustable voltage source V_s is used, and its value is changed until V_s=V_{diff}, namely until the metastable point lies on the line V_s=V_{diff}=$V_a - V_b$ (Fig. 5a).

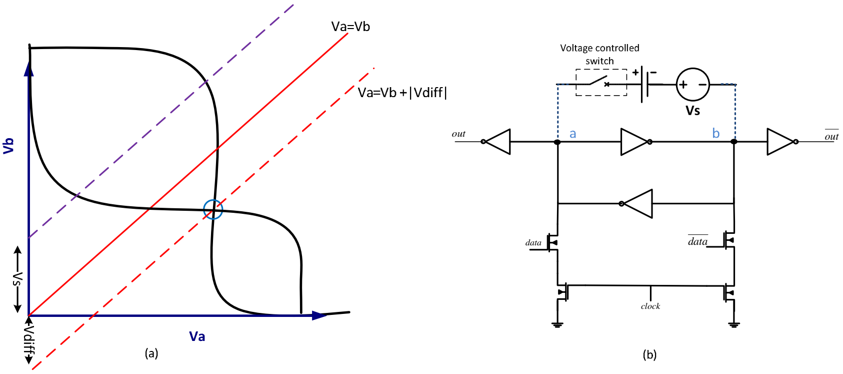

Fig. 5. Proposed technique for reaching metastability in asymmetric latches

We propose three different iterative algorithms to calculate V_{diff}:

- Current compensation (CC)
- Transient bisections (TB)

The current compensation algorithm adjusts the voltage V_S with the switch closed, using the circuit of Fig. 5b with an arbitrary initial value of V_s. If V_s>V_{diff}, current flows in one direction, and if V_s<V_{diff}, current flows in the opposite direction (Fig. 6). The algorithm iteratively adjusts V_S until the current is zero. At that stage,

$V_s = V_{diff}$ and the latch is metastable. A pseudo-code describing the algorithm is shown in Alg. 1. It starts with two initial voltages (V_{i+}, V_{i-}) yielding currents (I_s) with opposite sign. Then the algorithm performs a binary search untill the current falls below the desired error tolerance (ε). The value of V_{diff} is given by the last value of $(V_{i+} + V_{i-})/2$. The algorithm uses only SPICE DC simulations .

Algorithm 1. Calculate V_{diff} using CC

```
Require: $V_{i+}$ leads to $I_s \geq 0$
Require: $V_{i-}$ leads to $I_s < 0$
while $(|I_s| \geq \epsilon)$ do
    $V_s \leftarrow (V_{i+} + V_{i-})/2$
    $DC\_sim(V_s)$
    if $(I_s \geq 0)$ then
        $V_{i+} \leftarrow (V_{i+} + V_{i-})/2$
    else
        $V_{i-} \leftarrow (V_{i+} + V_{i-})/2$
    end if
end while
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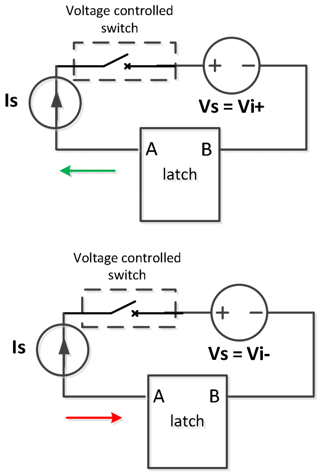

Fig. 6. Illustration of CC circuit diagram and behavior

In the transient bisection method, SPICE transient simulations are used with the circuit of Fig. 5b. The algorithm starts by choosing two values for V_s, $\{V_{i+}, V_{i-}\}$ which lead to two opposite transitions of the node V_a (or V_b). The transition direction is determined by the value of the voltage at the end time of the simulation (T). The transition settling time (T_S), measured from the time when the switch is released is computed, and the resolution is given by the maximum settling time allowed (MAX_{T_S}). Next, by binary search the algorithm finds a narrower interval, which also produces two opposite transitions on its extremes. A pseudo code for the algorithm is shown in Alg. 2

Algorithm 2. Calculate V_{diff} using TB

```
Require: $V_{i+}$ leads to $V_a(t = T) == V_{dd}$
Require: $V_{i-}$ leads to $V_a(t = T) == 0$
while $(T_s \leq MAX_{T_s})$ do
    $V_s \leftarrow (V_{i+} + V_{i-})/2$
    $transient\_sim(V_s)$
    if $(V_a(t = T) == V_{dd})$ then
        $V_{i+} \leftarrow (V_{i+} + V_{i-})/2$
    else
        $V_{i-} \leftarrow (V_{i+} + V_{i-})/2$
    end if
end while
```

Once the value of V_{diff} is found, with either one of these two methods, a single transient simulation is performed with the circuit of Fig. 5b. The voltage source V_s is set to the found value of V_{diff} and the switch is opened showing a divergence of the metastabale nodes. Re-writing Eq. (4) for the voltage node difference (v_D)

$$\begin{aligned}\underbrace{v_a(t) - v_b(t)}_{v_D(t)} + \underbrace{v_{ma} - v_{mb}}_{V_{diff}} &= (v_{1+} - v_{2+})e^{t/\tau} + (v_{1-} - v_{2-})e^{-t/\tau} \\ &\approx (v_{1+} - v_{2+})e^{t/\tau}\end{aligned} \tag{5}$$

The negative exponent term in Eq. (5) decreases fast with time and can be neglected. Fig. 7 shows a transient simulation of the circuit of Fig. 5 after finidng V_{diff} using the current compensation algorithm. As predicted in Eq. (5) the voltage ($v_D + V_{diff}$) shows exponential behavior and τ can be calculated from the slope of the blue curve (green line). When v_D is larger than about 100 mV the small signal model fails and the traces are no longer exponential as can be seen for times greater than 2.2nsec in Fig. 7.

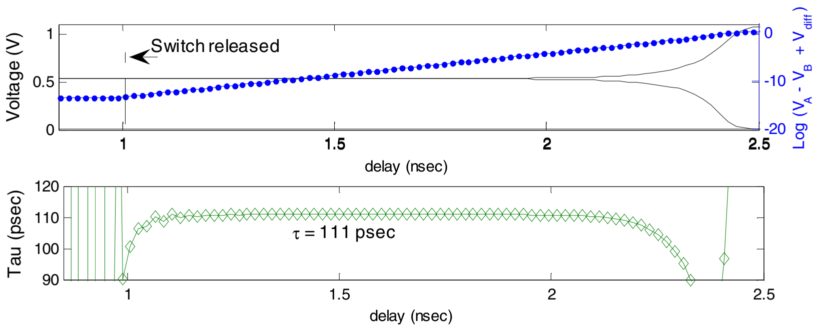

Fig. 7. Extended short node simulation for asymmetric latch using current compensation method to find V_{diff}

Though the two proposed methods generate consistent results for V_{diff} and hence for τ, the CC method incurs less computational effort and requires simpler simulations than the bisection method. CC method require DC simulations only, while TB requires several transient SPICE simulations with fine resolution and long run times. In order to achieve the same resolution for V_{diff} in the TB method, the transient simulation time in each run should be increased and hence increasing the overall simulation time. For that reason our tested ENSS uses CC to calculate V_{diff}. The ENSS using CC proposed is more time efficient than the sweep simulation method [8] since it requires fewer steps of much simpler DC simulations compared to several transient simulation, iterations and interpolations required in the sweep method.

3.1 Metastability Time Window T_W

The drawback of the ENSS method is its inability to simulate the parameter T_W, required in Eq. (1) to calculate failure probability. In most cases, however, knowing the value of τ is sufficient to reliably estimate the failure probability and a lower bound on MTBF can be found. Since T_W is the smallest data input arrival time window such that for all data toggling outside this window the settling time of the latch does not increase above its nominal value [9], then $T_W \leq t_{setup} + t_{hold} \leq T_C$. Then the error probability can be re-written as:

$$MTBF \geq \frac{e^{S/\tau}}{\left(t_{setup} + t_{hold}\right) \times F_C \times F_D} \geq \frac{e^{S/\tau}}{F_D} \qquad (6)$$

Both last terms of Eq. (6) are good lower bounds for the design of reliable synchronizers using the simulation method proposed to obtain τ.

3.2 Multi Stage Synchronizers

The method derived so far applies only to a single latch. The calculation of the failure probability of a synchronizer comprising multiple cascaded latch stages from its constituent latch parts is given in [10]. A detailed study using our enhanced method is out of the scope of this work and will be addressed in future publications.

4 Simulations and Measurements

A library latch (Fig. 8) has been implemented in a 65nm LP CMOS process. Its performance has been measured and the results are compared here to our simulations based on the ENSS method, as well as to results generated by two other state of the art simulation methods, the sweep simulation method [8] [9] and the parametric simulation method [10]. CC method for calculating V_{diff} is used. The library latch is asymmetric due to different loading of the two latch nodes. All simulations were performed using SPICE BSIM4 model level 54. The measurement method was described in [11]

A comparison of τ in measurements and simulations is presented graphically in Fig. 9 for different levels of supply voltage between 0.95V and 1.3V, at room temperature. Fig. 10 shows the percentage error difference between each of the simulation methods and the measurements results of τ. Note that all three methods yield consistent values for τ with a maximum error of 11.5% with respect to measured values. The results of the proposed simulation method (ENSS) fall within 3% of the results of the other methods tested.

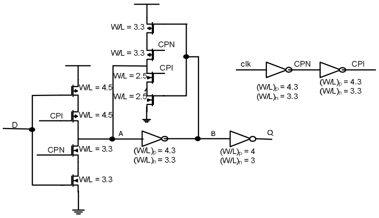

Fig. 8. Library latch used for simulation and measurements

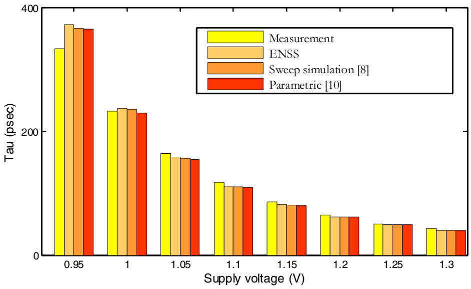

Fig. 9. $\boldsymbol{\tau}$ vs supply voltage, for measurements and simulations of a library 65nm CMOS FF

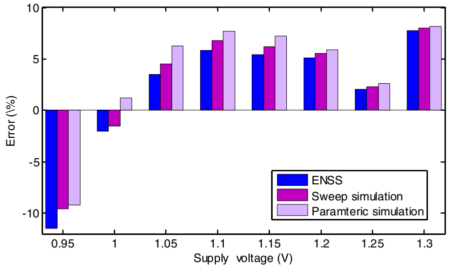

Fig. 10. Simulation errors with respect to measurements for different supply voltages

A comparison of the run times for ENSS simulation and the sweep simulation is shown in Fig. 11. For a fair comparison all simulations were performed using a common maximum resolution time (T_S). The V_{diff} resolution of ENSS was previously calibrated for T_S. This is why for higher supply voltages, for which τ is lower, more iterations are required to achieve the target resolution time and hence the run time is higher. The results show that our method provides accurate results much faster than the sweep and parametric method.

For the sake of completeness, Fig. 12 shows the offset of the metastable point from the symmetrical case, V_{diff}, against supply voltage. Note that V_{diff} is never zero along the range of supply voltage.

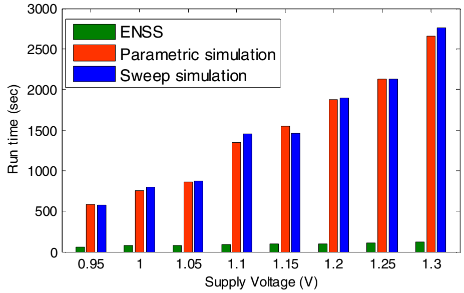

Fig. 11. Run times for ESNS simulation method and sweep simulation method

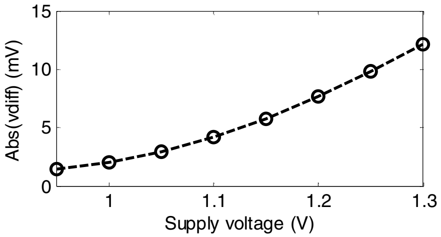

Fig. 12. Offset of metastable point ($\boldsymbol{V_{diff}}$) against supply voltage

5 Conclusions

We demonstrated that the node shorting simulation method as previously used in the literature is inappropriate for simulating latches and only works in the very special case of perfectly symmetric latches. We extended the node shorting simulation method for the case of non-symmetric latches and showed that it produced consistent results. The extended proposed method comprises two steps, finding the metastable offset voltage V_{diff} followed by a single run of a transient simulation. We showed two different algorithms to calculate V_{diff}, namely the current compensation, and the transient bisection method. We compared the results of our extended simulation method with the sweep and parametric simulation methods and showed that the results match with high accuracy but incurs less computation time and using only DC SPICE simulations followed by one transient simulation. We validated our simulation method against measurements taken on a circuit fabricated in a CMOS LP 65nm process. Simulation results predict τ with an error of less than 12% (measurement equipment error) compared to measurements, demonstrating that the proposed simulation method is suitable for characterizing synchronizers in a reliable and easy manner.

References

1. Kleeman, L., Cantoni, A.: Metastable behavior in Digital Systems. IEEE D&T 4(6), 4–19 (1987)
2. Dike, C., Burton, E.: Miller and noise effects in synchronizing flip-flop. JSSC 34(6), 849–855 (1999)
3. Beer, S., Ginosar, R., Priel, M., Dobkin, R., Kolodny, A.: The Devolution of Synchronizers. In: ASYNC 2010 (2010)
4. Chen, D., Singh, D., et al.: A comprehensive approach to modeling, characterizing and optimizing for metastability in FPGAs. In: FPGA 2010 (2010)
5. Zhou, J., Kinniment, D., Russell, G., Yakovlev, A.: Adapting synchronizers to the effects of on chip variability. In: ASYNC 2008 (2008)
6. Cox, J., Engel, G.L.: Metastability and Fatal System Errors. Blendics LLC (2010), http://www.blendics.com
7. Kinniment, D.: Synchronization and Arbitration in Digital Systems. Wiley (2007)
8. Yang, S., Greenstreet, M.: Computing synchronizer failure probabilities. In: DATE 2007 (2007)
9. Jones, I.W., Yang, S., Greenstreet, M.: Synchronizer Behavior and Analysis. In: ASYNC 2009 (2009)
10. Cox, J., Chaney, T., Zar, D.: Simulating the behavior of Synchronizers, white paper, http://www.blendics.com
11. Beer, S., et al.: An on-chip metastability measurement circuit to characterize synchronization behavior in 65nm. In: ISCAS (May 2011)
12. Kawaguchi, H., Sakurai, T.: A reduced clock-swing flip-flop (RCSFF) for 63% power reduction. IEEE J. Solid-State Circuits (May 1998)
13. Levacq, D., Yazid, M., et al.: Half VDD Clock-Swing Flip-Flop with Reduced Contention for up to 60% Power Saving in Clock Distribution. In: ESSCIRC (September 2007)